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PRODUCT CATALOG

Last Updated: November 2010

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RADAR & SDR I/O

RADAR & SDR I/O - PMC/XMC

MODEL	DESCRIPTION
7131	16-Channel Multiband Receiver with A/Ds and FPGA - PMC
7140	Dual Multiband Transceiver with FPGA - PMC/XMC
7140-420	Transceiver with Dual Wideband DDC and Interpolation Filter - PMC/XMC
7140-430	Transceiver with 256-Channel Narrowband DDC - PMC/XMC
7141	Dual Multiband Transceiver with FPGA - PMC/XMC
7141-703	Dual Multiband Transceiver with FPGA - Ruggedized PMC/XMC
7141-420	Transceiver with Dual Wideband DDC and Interpolation Filter - PMC/XMC
7141-430	Transceiver with 256-Channel Narrowband DDC - PMC/XMC
7142	Multichannel Transceiver with Virtex-4 FPGAs - PMC/XMC
7142-428	Transceiver with Four Multiband DDCs and Interpolation Filter - PMC/XMC
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC
7151	256-Channel DDC with four 200 MHz, 16-bit A/Ds - PMC
7152	32-Channel DDC with four 200 MHz, 16-bit A/Ds - PMC
7153	4/2-Channel DDC, four 200 MHz 16-bit A/Ds, Beamformer - PMC/XMC
7156	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC
7158	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC
Cobalt 71620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC
Cobalt 71621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC
Cobalt 71630	1 GHz A/D and D/A, Virtex-6 FPGA - XMC
Cobalt 71650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - XMC
Cobalt 71660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - XMC
Cobalt 71661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - XMC
	Customer Information

[RADAR & SDR I/O - CompactPCI](#)

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[RADAR & SDR I/O - 3U VPX](#)

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Features

- Two 80 or 105 MHz, 14-bit A/D converters
- 16 channels of multiband digital downconverters
- 5 kHz to 10 MHz output bandwidth for $f_s = 100$ MHz
- 250 MHz input bandwidth
- Ideal for IF sampling
- User-configurable Xilinx Virtex-II FPGA
- Custom FPGA I/O through the P4 PMC connector
- Bypass path allows direct capture of A/D data
- Front panel clock and sync bus
- Synchronization of up to 80 modules (with Model 9190)
- **Ruggedized version available: 7131-702**

General Information

Model 7131 is a general-purpose 16-channel multiband digital receiver PMC module which attaches directly to PMC-compatible baseboards. It includes both a Virtex-II FPGA and two 14-bit A/Ds for signal processing.

Front End

The Model 7131 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors.

The two inputs are transformer coupled and digitized by AD6645 14-bit A/D converters. The AD6645 operates at a maximum sampling rate of 80 MHz in the standard unit and up to 105 MHz for option -100.

The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, or from an external sample clock supplied through a front panel SMA connector or the front panel sync bus.

Digital Downconverters

The 7131 includes four TI/Graychip GC4016 quad multiband digital downconverter chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable channels capable of center frequency tuning from DC to $f_s/2$, where f_s is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from the two A/D converters. A cross-bar switch in each GC4016 allows all 16 channels on the board to select either of the two A/D inputs for flexible switching.

Output Bandwidth

With a 100 MHz sample clock, the useable output bandwidth of each of the downconverter channels is 2.5 MHz. However, since the Model 7131 delivers parallel digital outputs from the GC4016 into the FPGA, users can take advantage of the GC4016 channel combining mode to join two or four channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.

Since both A/D converters connect directly to the FPGAs, signals with even wider bandwidths can be accommodated.

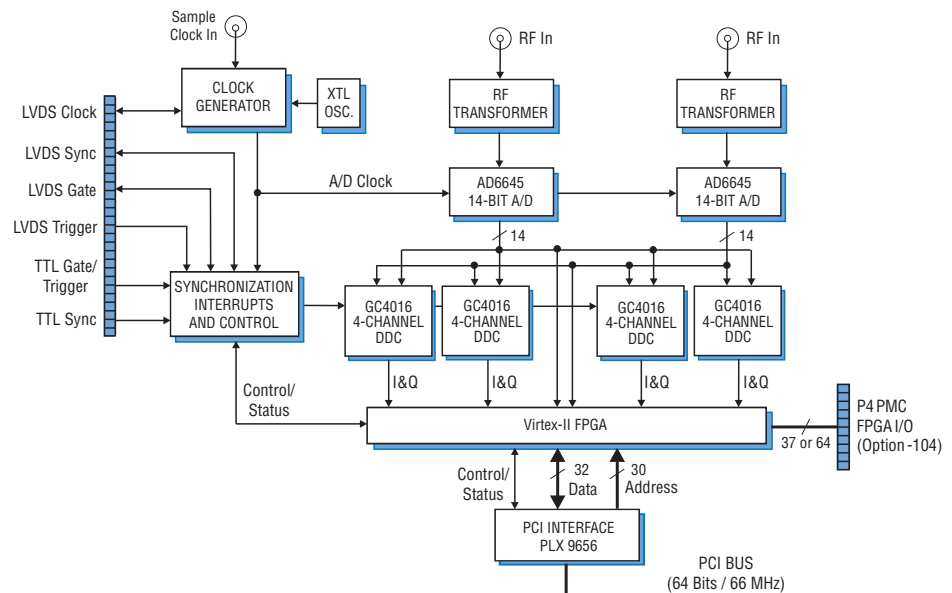
FPGA

The downconverter outputs are delivered to a Xilinx Virtex-II XC2V1000 FPGA (XC2V3000 with option -300) which is factory configured to perform various modes of data packing, formatting and channel selection.

Dual port memories in the FPGA provide efficient PCI Bus transfers by buffering receiver and A/D data.

The A/D outputs are also connected directly to the FPGA so that wideband A/D data can be delivered directly to the baseboard bypassing the downconverters. An A/D decimation mode allows one of every N samples to be written into the FPGA memory, where N is any integer between 1 and 4096. This overcomes the lower frequency limit on the A/D sample clock.

Option -104 installs the P4 PMC connector with 37 or 64 signal line connections to the XC2V1000 or XC2V3000 FPGA respectively, for custom I/O through P4. ➤



Ruggedization

Model 7131-702 meets Pentek Ruggedization Level L2 requirements by extending the operating and storage temperature range of the commercial version and by adding resistance to shock and vibration.

Environmental Specifications, Option -702

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Sine Vibration: 2 g, 20–500 Hz

Random Vibration: 0.04 g²/Hz, 20–2,000 Hz

Shock: 20 g, 11 msec

Relative Humidity: 0 to 95%, non-condensing;

With Option -720: conformal coating, 0 to 100% non-condensing

Ordering Information

Model	Description
7131	16-Channel Multiband Receiver with A/Ds and FPGA - PMC
Options:	
-100	105 MHz A/D with 100 MHz crystal oscillator
-104	FPGA I/O with the P4 connector
-300	XC2V3000 FPGA
-702	Pentek Level 2 Ruggedization
-720	Conformal coating

Synchronization

The front panel clock and sync bus allow one 7131 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple 7131's.

Up to eight slave 7131 modules can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator. In addition to the LVDS timing bus, the Model 7131 can receive front panel TTL input signals for gate or trigger functions.

Interrupt Sources

The Model 7131 has several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload output codes, transitions on the gate signals, clock loss, buffer swapping, or a programmable over-temperature condition or faulty power supply voltage. The ADM1024 Voltage/Temperature Monitor provides constant monitoring of critical voltages and temperatures and generates an interrupt if values exceed threshold limits which are user programmable over the PCI interface.

PCI Interface

The FPGA output is connected to a 66 MHz, 64-bit PCI interface capable of 528 MB/sec peak data rates. An industry standard PLX9656 PCI interface chip ensures full conformance to all PCI bus timing specifications.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMA connectors

Transformer Type: Mini-Circuits ADT4-6T

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 270 MHz

A/D Converters, Standard

Type: Analog Devices AD6645-80

Sampling Rate: 30 MHz to 80 MHz

Internal Clock: 80 MHz crystal osc.

External Clock: 30 to 80 MHz

Resolution: 14 bits

A/D Converters, Option -100

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: 100 MHz crystal osc.

External Clock: 30 to 105 MHz

Resolution: 14 bits

Clock Source: Onboard crystal oscillator, front panel ext clock, or LVDS clock

External Clock

Type: Front panel female SMA connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms impedance

Sync/Gate Bus

Type: 26-pin connector, with one clock, one sync, and two gate input/output LVDS signals; two trigger LVDS inputs; and one sync and one gate input TTL signals

Digital Downconverters

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D outputs are connected to all GC4016's

Output: Parallel complex data

Bypass Mode: Data from the A/D converters can be written directly into the FPGAs at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096

Field Programmable Gate Array

Type: Xilinx Virtex-II XC2V1000 standard

Option -300: Virtex-II XC2V3000

Option -104: Installs the P4 connector with 37 lines to the XC2V1000 or 64 lines to the XC2V3000 FPGA

Dual Port RAM Data Buffers

Size: 4k x 32 DPRAM expandable to 8k x 32 with option -300 FPGA

PCI Interface

Type: PLX Technology PCI 9656

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus (FPGA): 32-bit, 66 MHz

Data Transfer Modes: Direct slave mode and DMA mode

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.



Commercial version shown; ruggedized and conduction-cooled versions also available.



Features

- Complete software radio transceiver solution
- VITA 42.0 XMC compatible with switched fabric interfaces
- Two 105 MHz 14-bit A/Ds
- Input signal bandwidth: 40 MHz
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on P4
- Optional factory-installed IP Cores available
- **Ruggedized and conduction-cooled versions available**

General Information

Model 7140 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters capable of bandwidths to 40 MHz and above. The Model 7140 uses the popular PMC format and supports the emerging VITA 42 XMC standard with optional switched fabric interfaces.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel MMCX connectors at +4 dBm into 50 ohms with transformer coupling into AD6645 14-bit 105 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

A TI/Graychip GC4016 quad digital downconverter accepts either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter (DUC) and dual D/A accepts baseband real or complex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGA

The Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverter, digital upconverter and D/A converters.

Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

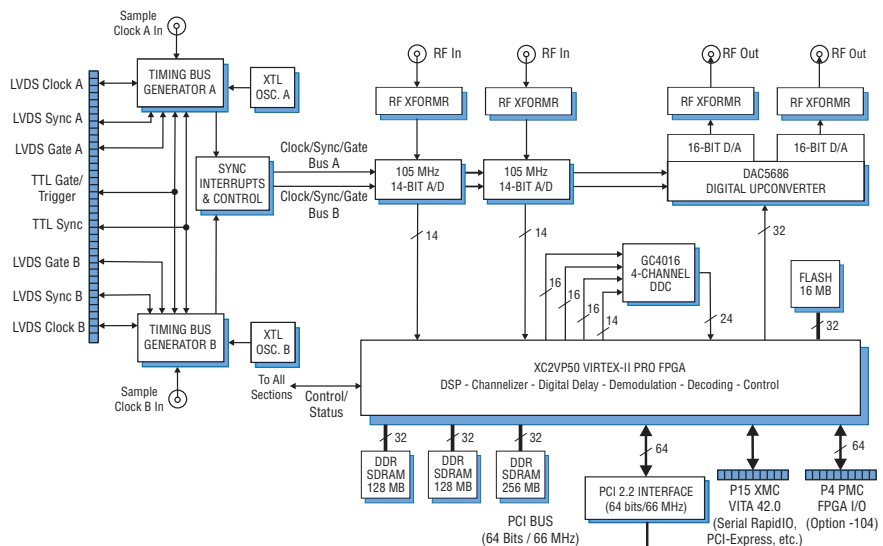
Option -104 adds the P4 PMC connector with 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O.

The FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As. ➤



XMC Interface

The Model 7140 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7140 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

Clocking and Synchronization

Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7140's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Interface

The Model 7140 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 270 MHz

A/D Converters

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 30 to 105 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

Option -002: -2 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -104: Installs P4 connector with 64 lines to the XC2VP50 FPGA

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7140	Dual Multiband Transceiver with FPGA - PMC/XMC
Options:	
-002	Full-Scale Output: -2 dBm into 50 ohms; 3 dB Passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through P4 connector
-420	Dual wideband DDC and digital interpolation filter cores, factory-installed
-430	256-channel narrowband DDC core, factory-installed
-5xx	XMC interface
-70x	Ruggedized & conduction-cooled versions



Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz

General Information

Model 7140-420, Dual Digital Transceiver with Wideband DDC and Interpolation Filter cores, is a complete software radio system in PMC/XMC format. It includes two A/D and two D/A converters for connecting to HF or IF ports of a communications or radar system.

The 7140 receiver section features two AD6645 105 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, the module includes Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 downconverter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The

NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

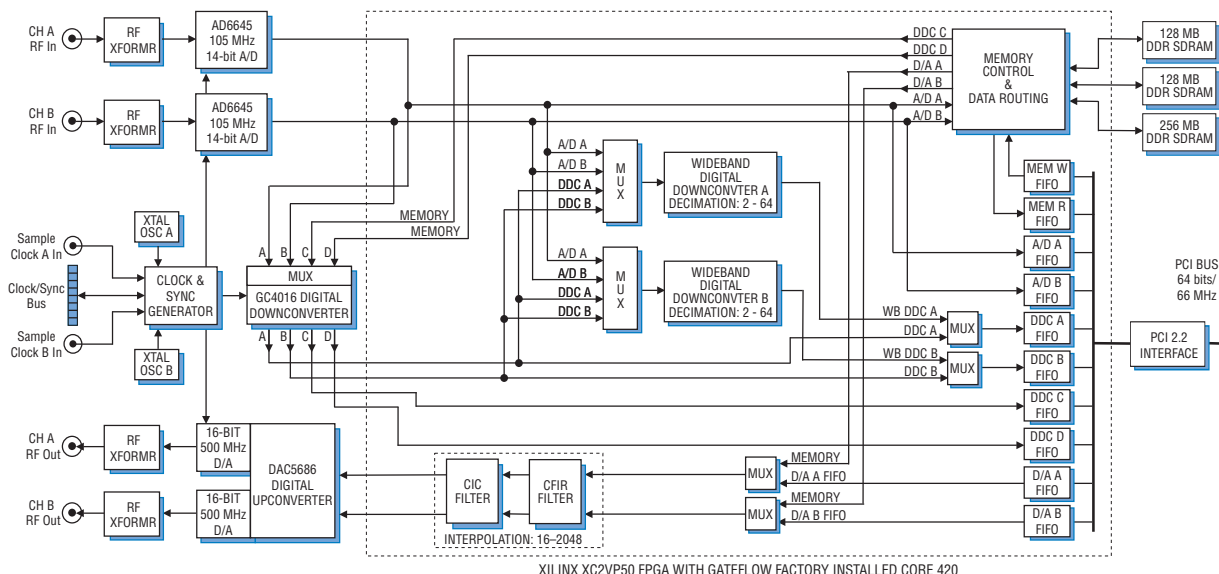
Two identical Core 420 DDCs are factory installed in the 7140 FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of the 7140 are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤



XMC Interface

The Model 7140-420 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7140 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As.

Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7140-420's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Interface

The Model 7140-420 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 270 MHz

A/D Converters

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 30 to 105 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz

max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7140-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - PMC/XMC

Contact Pentek for available options



Features

- Complete software radio transceiver solution
- GateFlow Core 430 with 256 channels of narrowband digital downconverters factory-installed
- 256 fully programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

General Information

Model 7140-430, Dual Digital Transceiver with 256-Channel Narrowband DDC Core 430, is a complete software radio system in a PMC/XMC module. It includes two A/D and two D/A converters for connection to HF or IF ports of a communications or radar system.

The 7140-430 receiver section features two AD6645 105 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7140-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

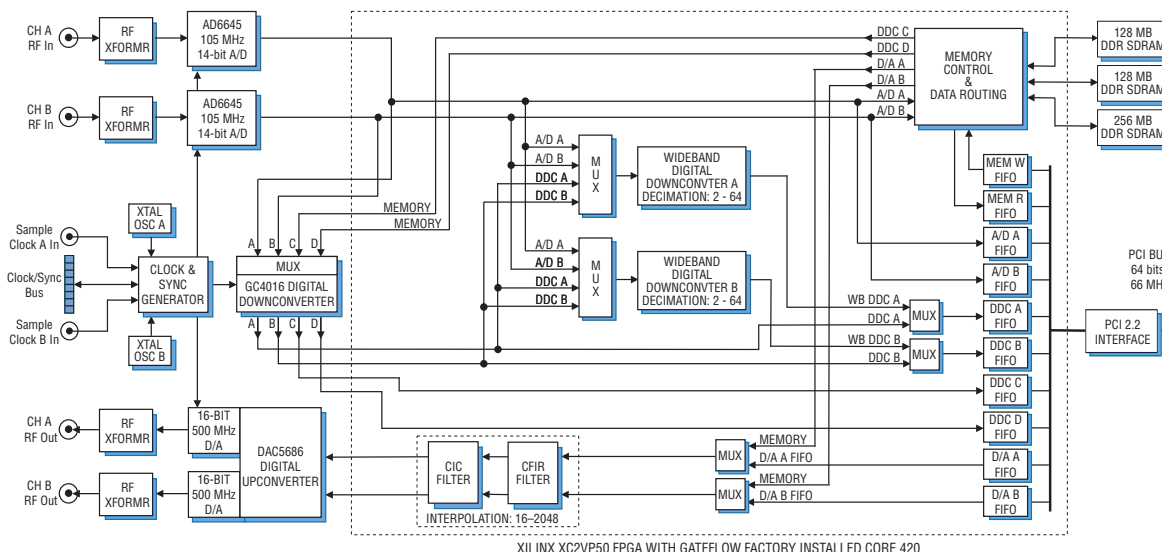
Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2 ³²
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in the Model 7140-430. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 40 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤



XMC Interface

The Model 7140-430 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7140-430 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As.

Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7140-430's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Interface

The Model 7140-430 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 270 MHz

A/D Converters

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 30 to 105 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7140-430	GateFlow Transceiver with 256-Channel Narrowband DDC Core factory-installed - PMC/XMC

Contact Pentek for available options



Commercial version shown; ruggedized and conduction-cooled versions also available.



Features

- Complete software radio transceiver solutions
- VITA 42.0 XMC compatible with switched fabric interfaces
- Two 125 MHz 14-bit A/Ds
- Input signal bandwidth: 50 MHz
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on P4
- Optional factory-installed IP Cores available
- ***Ruggedized and conduction-cooled versions available***

General Information

Model 7141 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters capable of bandwidths to 50 MHz and above. The 7141 uses the popular PMC format and supports the emerging VITA 42 XMC standard with optional switched fabric interfaces.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling for the LTC2255 14-bit 125MHz A/Ds.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

A TI/Graychip GC4016 quad digital downconverter accepts either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter (DUC) and dual D/A accepts baseband real or complex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGA

The Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverter, digital upconverter and D/A converters.

Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

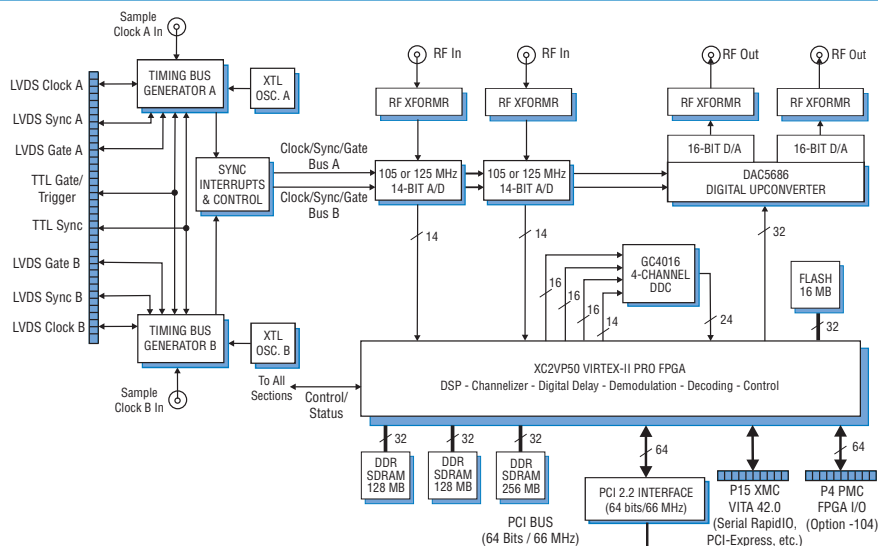
Option -104 adds the P4 PMC connector with 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O.

The FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As. ►



XMC Interface

Model 7141 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7141 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

Ordering Information

Model	Description
7141	Dual Multiband Transceiver with FPGA - PMC/XMC
Options:	
-002	Full-scale output: -2 dBm into 50 ohms; 3 dB passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through P4 connector
-125	125 MHz Bus A and 100 MHz Bus B internal oscillators
-420	Dual wideband DDC and digital interpolation filter cores, factory-installed
-430	256-channel narrowband DDC core, factory-installed
-5xx	XMC interface
-70x	Ruggedized & conduction-cooled versions

► Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7141's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

The SDRAMs are also available as a resource for the PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Interface

Model 7141 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

Option -002: -2 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -104: Installs P4 connector with 64 lines to the XC2VP50 FPGA

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.



Features

- Complete software radio transceiver solution
- VITA 42.0 XMC compatible
- Two 125 MHz 14-bit A/Ds
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 28 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on P4
- Optional factory-installed IP Cores available

General Information

Model 7141-703 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters capable of bandwidths to 40 MHz and above. The Model 7141-703 uses the popular PMC format and supports the emerging VITA 42 XMC standard with optional switched fabric interfaces. The Model 7141-703 is offered as a fully conduction-cooled/ruggedized board meeting Pentek's L3 ruggedization level (option 703).

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

A TI/Graychip GC4016 quad digital downconverter accepts either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter (DUC) and dual D/A accepts baseband real or complex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel SSMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGA

The Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverter, digital upconverter, and D/A converters.

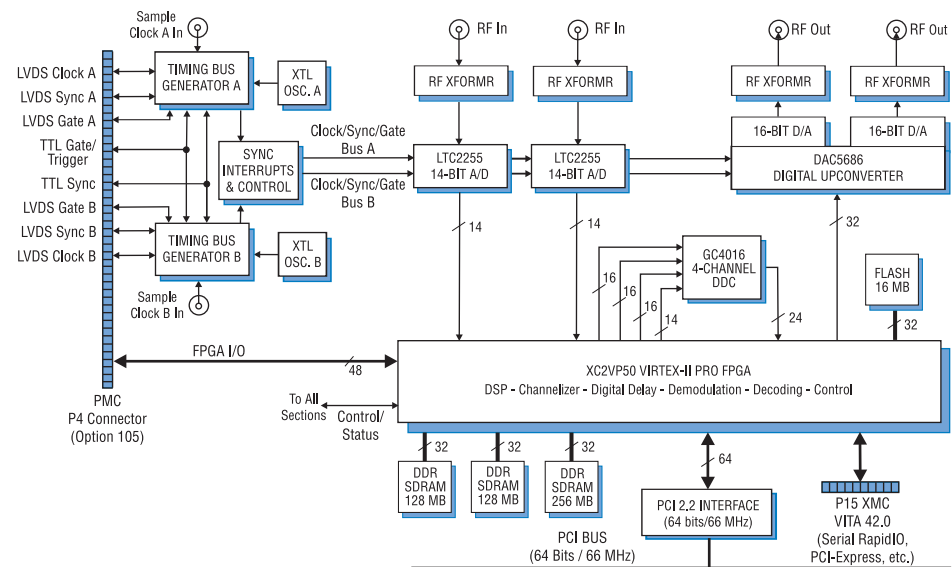
Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

Option -105 adds the P4 PMC connector with 28 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O.

The FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals. ➤



XMC Interface

The Model 7141-703, option 520 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard defines a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board.

With two 4X links, the 7141-703 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and can support switched fabric protocols such as Serial RapidIO and PCI Express.

Software Support

The Pentek ReadyFlow Board Support Package and VxWorks, Linux and Windows device drivers for specific embedded processor boards and operating systems, speed software development tasks.

The Pentek GateFlow FPGA Design Kit facilitates user-installed FPGA functions using the Xilinx ISE Foundation tool suite. The FPGA Design Kit allows the user to configure FPGAs for implementing preprocessing functions such as convolution, framing, pattern recognition or decompression.

Ordering Information

Model	Description
7141	Multiband Transceiver with FPGA - PMC/XMC
Options:	
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B internal oscillators
-125	125 MHz Bus A and 100 MHz Bus B oscillators
-105	FPGA I/O and sync bus through P4 connector
-5xx	XMC interface
-703	Level L3 - Ruggedized & conduction-cooled version

► Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the down-converter, the upconverter, and the D/As. Both timing buses accept clocks from two external reference clocks or two internal oscillators.

Timing signals for both Bus A and B are available on the P4 PMC connector allowing multiple modules to be synchronized. In the slave mode, differential LVDS inputs drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7141-703's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Interface

The Model 7141-703 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

External Clock: 1 to 125 MHz

Resolution: 14 bits

Clock Source: Timing Bus A or B

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMCX connectors

Full Scale Output: +4 dBm into 50 ohms (other options available)

3 dB Passband: 60 kHz to 300 MHz (other options available)

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Source: Timing Bus A or B

Timing Buses A & B: Clocks selectable from onboard crystal oscillators, external or LVDS bus, gates and syncs from LVDS bus

External Clocks: Front panel female SSMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

P4 Timing Bus: Available as option 105, dual clock/sync/gate input/output LVDS buses; one sync TTL input, one gate TTL input

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -105: Installs P4 connector with 56 lines to the XC2VP50 FPGA

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Level L3):

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Sine Vibration: 10 g, 20-2000 Hz

Random Vibration: 0.1 g²/Hz, 20-2,000 Hz

Shock: 30 g, 11 msec

Relative Humidity: 0 to 95%, non-condensing; 0 to 100% with conformal coating



Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz
- **Conduction-cooled version available with Model 7141-703**

General Information

Model 7141-420, Dual Digital Transceiver with Wideband DDC and Interpolation Filter cores, is a complete software radio system in PMC/XMC format. It includes two A/D and two D/A converters for connecting to HF or IF ports of a communications or radar system.

The 7141-420 receiver section features two LTC2255 125 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGA and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, the module includes Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 down-converter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The

NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

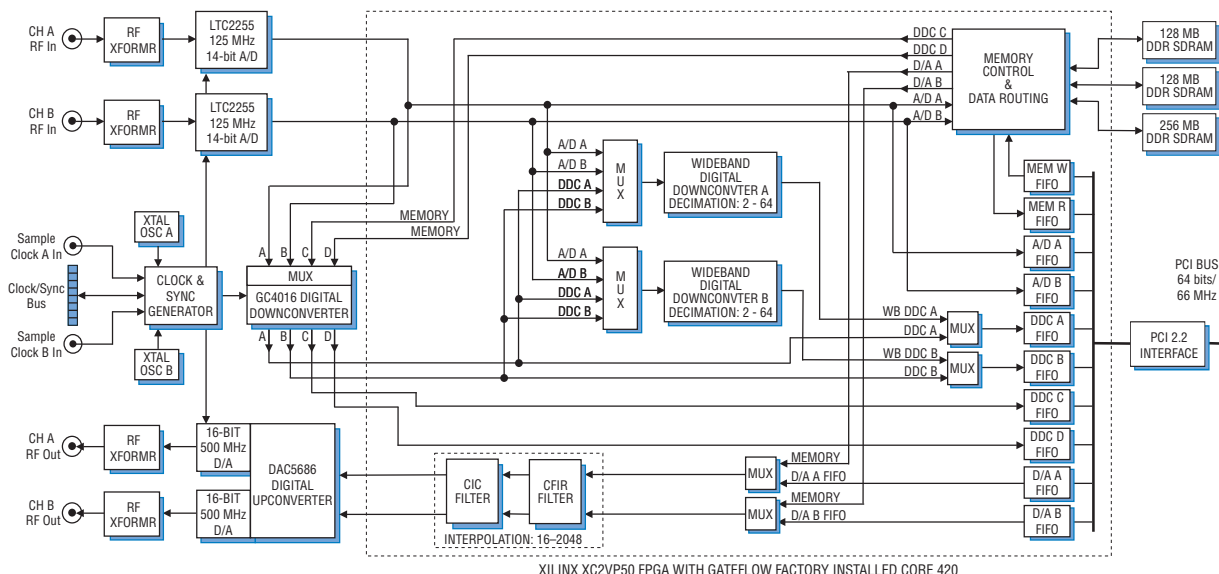
Two identical Core 420 DDCs are factory installed in the 7141-420 FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 16,384 which matches the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of the 7141-420 are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤



XMC Interface

Model 7141-420 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7141-420 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As.

Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7141-420's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

PCI Interface

Model 7141-420 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7141-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - PMC/XMC

Contact Pentek for available options



Features

- Complete software radio transceiver solution
- GateFlow Core 430 with 256 Channels of Narrowband Digital Downconverters factory-installed
- 256 fully programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256
- **Conduction-cooled version available with Model 7141-703**

General Information

Model 7141-430, Dual Digital Transceiver with 256-Channel Narrowband DDC Core 430, is a complete software radio system in a PMC/XMC module. It includes two A/D and two D/A converters for connection to HF or IF ports of a communications or radar system.

The 7141 receiver section features two LTC2255 125 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7141-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

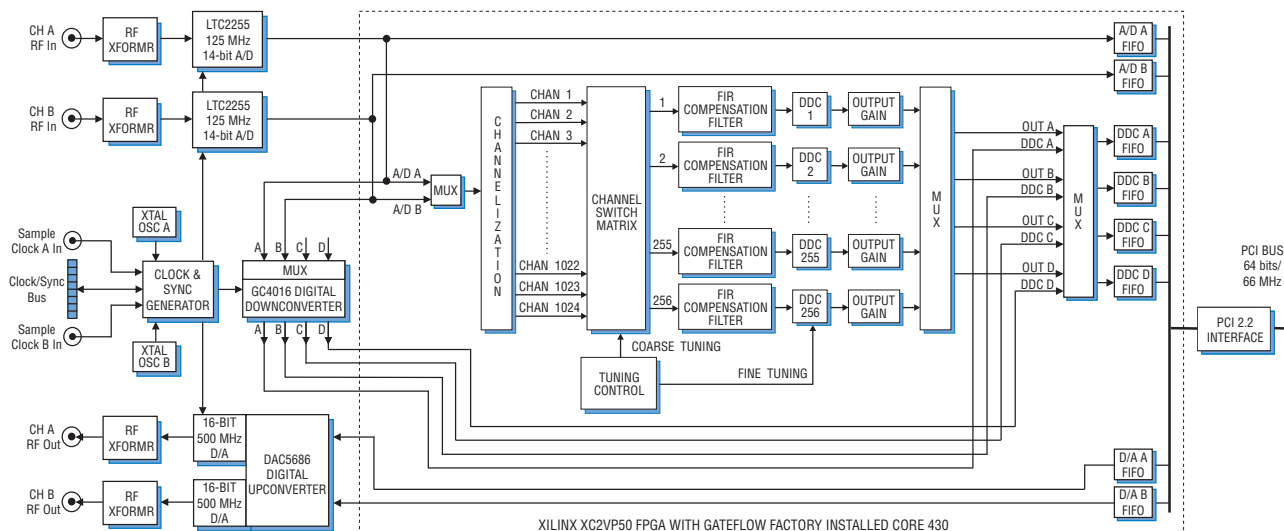
Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2^{32}
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in the Model 7141-430. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any interger value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤



XMC Interface

Model 7141-430 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7141-430 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As.

Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7141-430's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

PCI Interface

Model 7141-430 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7141-430	GateFlow Transceiver with 256-Channel Narrowband DDC Core factory installed - PMC/XMC

Contact Pentek for available options



Features

- Complete software radio interface solution
- VITA 42.0 XMC compatible with switched fabric interfaces
- Four 125 MHz 14-bit A/Ds
- One digital upconverter
- One 500 MHz 16-bit D/A
- 768 MB of DDR2 SDRAM
- Xilinx Virtex-4 FPGAs
- Up to 2.0 seconds of delay or data capture at 125 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multimodule synchronization
- 32 pairs of LVDS connections to the Virtex-4 FPGA for custom I/O
- Optional factory-installed IP Cores available

General Information

Model 7142 is a multichannel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds and one upconverter and D/A converter capable of bandwidths to 50 MHz and above. The Model 7142 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched fabric interfaces.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

The Model 7142 architecture includes two Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can include their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

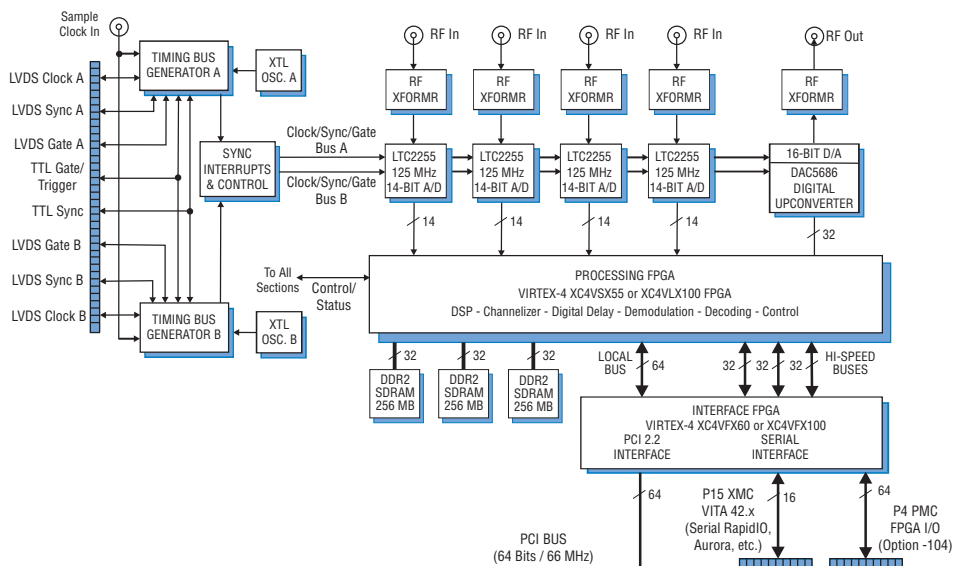
The Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission.

For applications requiring more FPGA logic cells, the Model 7142 can be optionally configured with an XC4VLX100 in place of the XC2VSX55 for 110,592 logic cells.

A second Virtex-4 FPGA provides board interfaces including PCI and serial I/O. The XC4VFX60 FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. The Model 7142 can be optionally configured with an XC4VFX100 in place of the XC4VFX60.

Option -104 installs the P4 PMC connector with 32 pairs of LVDS connections to the XC4VFX60/100 FPGA for custom I/O. ▶



XMC Interface

The Model 7142 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7142 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds and the upconverter and the D/A. Two internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7142s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

The Model 7142 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal osc.

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms (other options available)

3 dB Passband: 60 kHz to 300 MHz (other options available)

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: One Xilinx Virtex-4 XC4VSX55 & one Xilinx Virtex-4 XC4VFX60

Option -100: XC4VFX100 replaces XC4VFX60

Option -110: XC4VLX100 replaces XC4VSX55

Custom I/O

Option -104: Installs the P4 connector with 64 lines to the XC4VFX60/100 FPGA

Memory

DDR2 SDRAM: 768 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

7142 Multichannel Transceiver with Virtex-4 FPGAs - PMC/XMC

Options:

-100 XC4VFX100 replaces XC4VFX60
-104 FPGA I/O through the P4 connector
-110 XC4VLX100 replaces XC4VSX55
-428 Four multiband DDCs and interpolation filter, factory-installed core
-5xx XMC interface



Features

- Complete software radio transceiver solution
- GateFlow IP Core 428, with four high-performance multiband DDCs and Interpolation Filter, factory-installed
- Improved dynamic range
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4

General Information

Model 7142-428, Digital Transceiver with Multiband DDC and Interpolation Filter core, is a complete software radio system in a PMC/XMC module. It includes four A/D and one D/A converters capable of bandwidths to 40 MHz and above for connection to HF or IF ports of a communications or radar system.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other module resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating

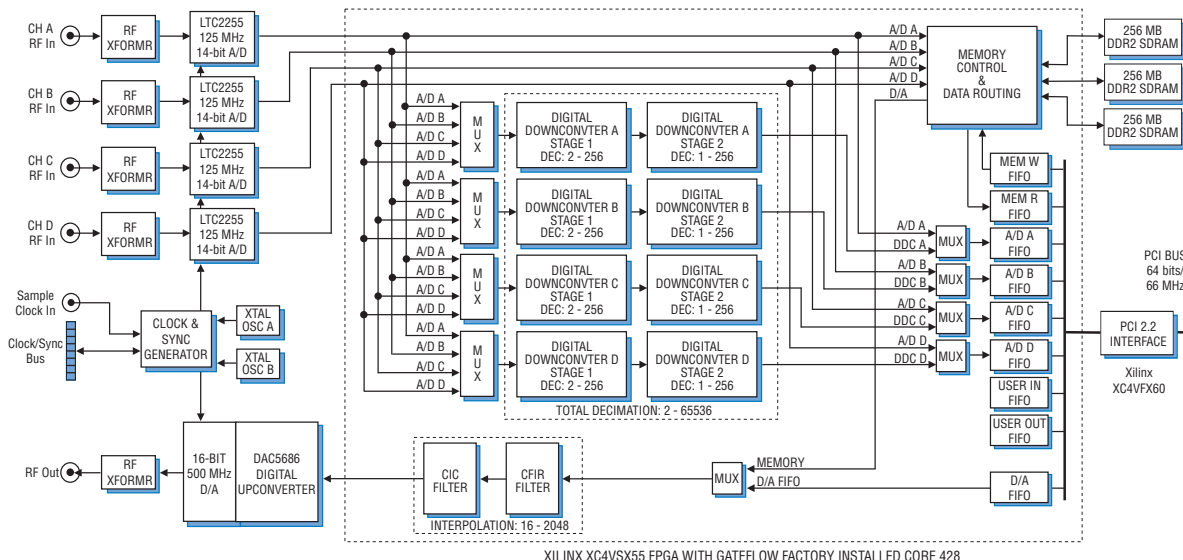
FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ➤



XMC Interface

The Model 7142-428 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7142-428 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds and the upconverter and the D/A. Two internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7142-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

PCI Interface

The Model 7142-428 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal osc.

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: One Xilinx Virtex-4 XC4VSX55 and one Xilinx Virtex-4 XC4VFX60

Memory

DDR2 SDRAM: 768 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7142-428	Gateflow Transceiver with four DDCs and Interpolation Filter factory-installed - PMC/XMC

Contact Pentek for available options

New!

Model 7150

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC



Features

- Complete software radio interface solution
- VITA 42.0 XMC compatible with switched fabric interfaces
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources ideally matched to the requirements of high-performance systems.

Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched-fabric interfaces.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The Model 7150 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters,

DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

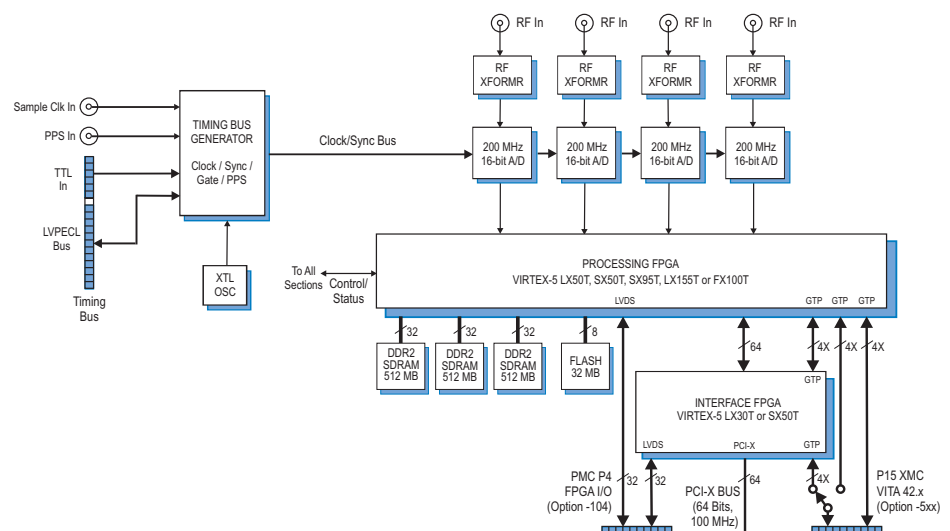
The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7150 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs the P4 PMC connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

The Model 7150 architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ➤



XMC Interface

The Model 7150 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides serial data links with up to 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7150 achieves up to 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7150s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. More modules can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI-X Interface

The Model 7150 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66, 100 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, the Model 7150 can be optionally factory-configured with x4 PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs P4 connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC
Options:	
-104	FPGA I/O through the P4 connector
-5xx	XMC interface

Contact Pentek for additional available options.



Features

- 256 channels of DDC
- Four 200 MHz 16-bit A/Ds
- Independent tuning for each channel
- DDC decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization



General Information

Model 7151 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 256-channel installed DDC (digital downconverter) IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

Model 7151 uses the industry standard PMC daughtercard format compatible with numerous carrier boards for VME, PCI, and CompactPCI.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7151 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 256 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

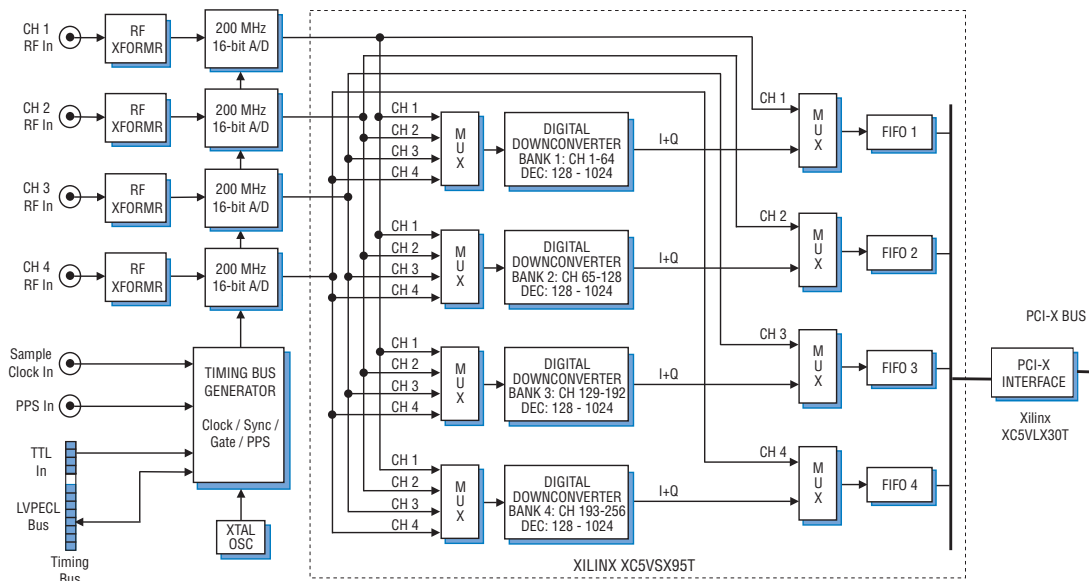
The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wide-band A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI-X bus. ➤



► Clocking and Synchronization

The Model 7151 architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7151s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. More modules can be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7151 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33, 66 and 133 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface

PCI-X Bus: 64-bits, 133 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp:

Standard: 0° to 50° C

L2 Extended Temp (Option -702):
-20° to 65° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7151	256-Channel DDC with four 200 MHz, 16-bit A/Ds - PMC

Options:

-702	L2 Extended temperature operation
-730	Two-slot heat sink

Contact Pentek for additional available options.

New!

Model 7152

32-Channel DDC with four 200 MHz, 16-bit A/Ds - PMC



Features

- 32 channels of DDC in four banks of 8 channels
- Four 200 MHz, 16-bit A/Ds
- Independent 32-bit DDC tuning for all 32 channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths from 20 kHz to 10 MHz
- Common decimation factor within each DDC bank
- Different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multimodule synchronization



General Information

Model 7152 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 32-channel installed DDC (digital downconverter) IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

Model 7152 uses the industry standard PMC daughtercard format compatible with numerous carrier boards for VME, PCI, and CompactPCI.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7152 employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 32 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

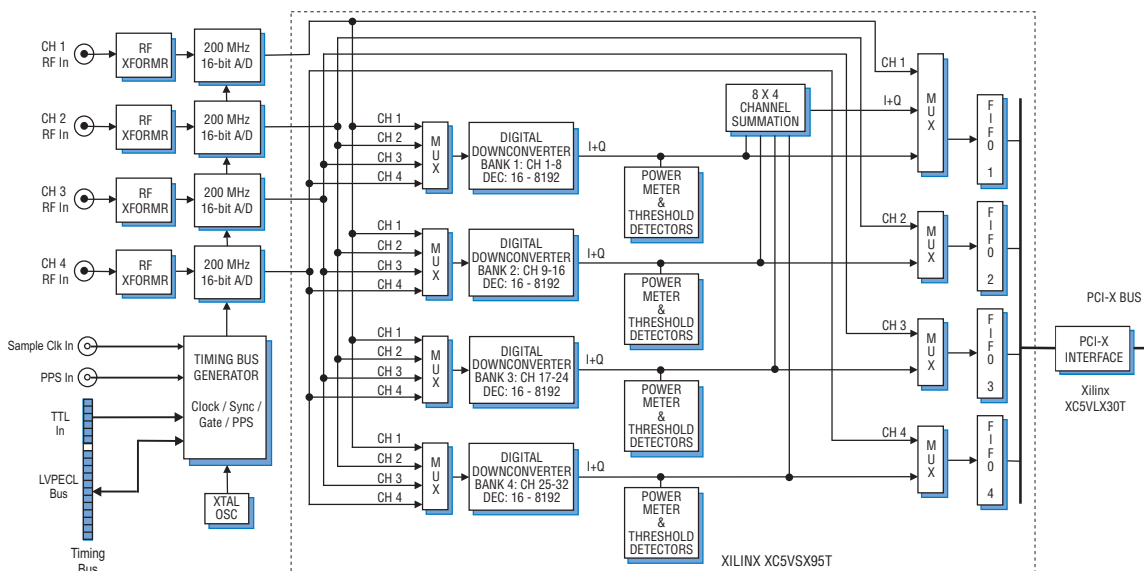
All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

The 7152 features 32 power meters that continuously measure the individual average power output of each of the 32 DDC channels. The time constant of the averaging interval for each meter is programmable up to 16K samples. In addition, 32 threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤



► Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI-X bus.

Clocking and Synchronization

The Model 7152 architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7152s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. For larger systems, many more modules can be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7152 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7152	32-Channel DDC with four 200 MHz, 16-bit A/Ds - PMC

Options:

-730	Two-slot heat sink

Contact Pentek for additional available options.

New!

Model 7153

4/2-Ch. DDC, four 200 MHz 16-bit A/Ds, Beamformer - PMC/XMC



ReadyFlow
Board Support Package

Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- Four 200 MHz, 16-bit A/Ds
- 2 or 4 Channels of DDC
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7153 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

Model 7153 uses the industry standard PMC daughtercard format compatible with numerous carrier boards for VME, PCI, and CompactPCI.

A/D Converter Stage

The front end accepts four full scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling to four Texas Instruments ADS5485 200 MHz, 16-bit A/Ds.

The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7153 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sampling frequency.

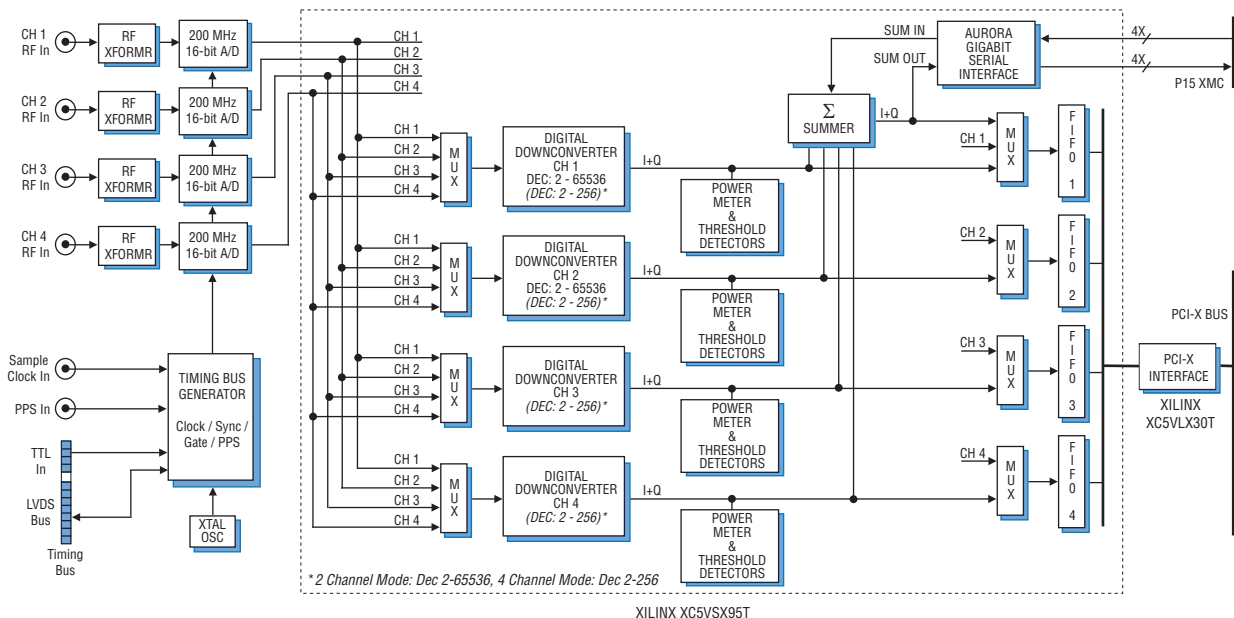
Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N .

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications. ➤



XMC Interface

The Model 7153 complies with the VITA 42.0 XMC specification. This standard provides serial data links between the XMC module and the carrier board. The 7153 beamformer architecture uses this link to create a board-to-board summation expansion chain for creating larger multichannel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

► Beamformer

In addition to the A/Ds and DDCs, the 7153 includes essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable-gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCI-X bus.

For larger systems, multiple 7153's can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates an x4 sum output stream to the next board through the P15 XMC connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the channels and to enable efficient block transfers to the PCI-X bus.

Clocking and Synchronization

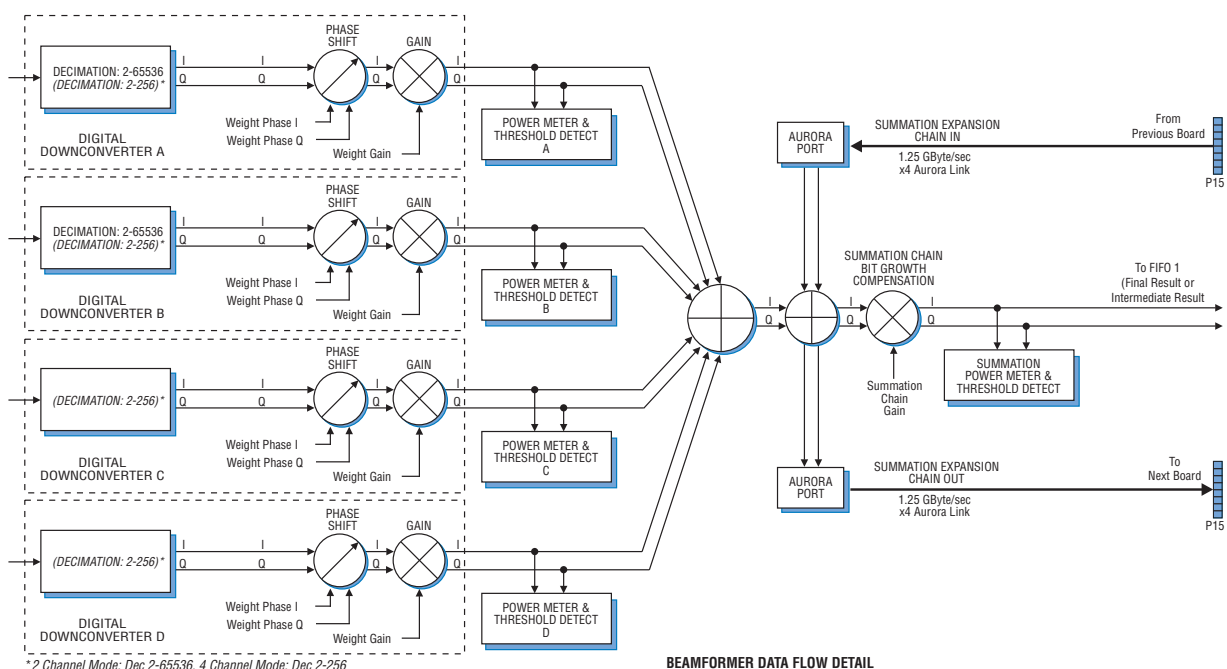
The Model 7153 architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven from the internal crystal oscillator, a front panel reference or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7153's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. More modules may be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7153 includes an industry-standard PCI-X interface. The interface includes four separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.



Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillator, external reference or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS, input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Digital Downconverter

Type: IP core for Xilinx Virtex-5

Qty of DDC Channels: 2 or 4

Center Frequency Tuning: 4 tuning words, one for each DDC channel

Center Frequency Tuning Range: DC to f_s with 32 bit resolution

NCO SFDR: -120 dBFS

Channel Phase Offset Adjustment: 32-bit resolution

Channel Gain Adjustment: 32-bit resolution

Input Selection for DDC Banks: Any channel can select any of the four A/Ds

Decimation Range (N):

2-Channel Mode: 2 to 65536

4-Channel Mode: 2 to 256

FIR Filter: Default passband $0.8 \cdot f_s / N$ with 0.2 dB passband ripple and 100 dB adjacent channel rejection

FIR Filter Coefficients: 18 bits, user-programmable (default values provided)

Qty FIR Filter Taps: $28 \cdot N / 8$

Output Format: 24 bits I + 24 bits Q

Output Spectrum Modes: Normal or frequency-reversed

Output Spectrum Offset: No offset or offset by one-half the output bandwidth

Beamformer

Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain

Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion: 32-bit

Output Multiplexer and FIFO

Qty Output FIFOs: Four

FIFO Source Selection: Independent multiplexer selects DDC output or A/D

PCI Interface

Type: IP core in Xilinx FPGA

PCI-X Bus: 64 bits, 100 MHz and 64 or 32 bits at 33 or 66 MHz

DMA: 4-channel demand mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7153	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - PMC/XMC

Options:

-730	Two-slot heat sink

Contact Pentek for available options.

New!

Model 7156

Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC



Features

- Complete software radio interface solution
- Two 400 MHz, 14-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O on P14

General Information

Model 7156 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters, two Virtex-5 FPGAs and two banks of DDR2 SDRAM. The Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing, data capture or routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

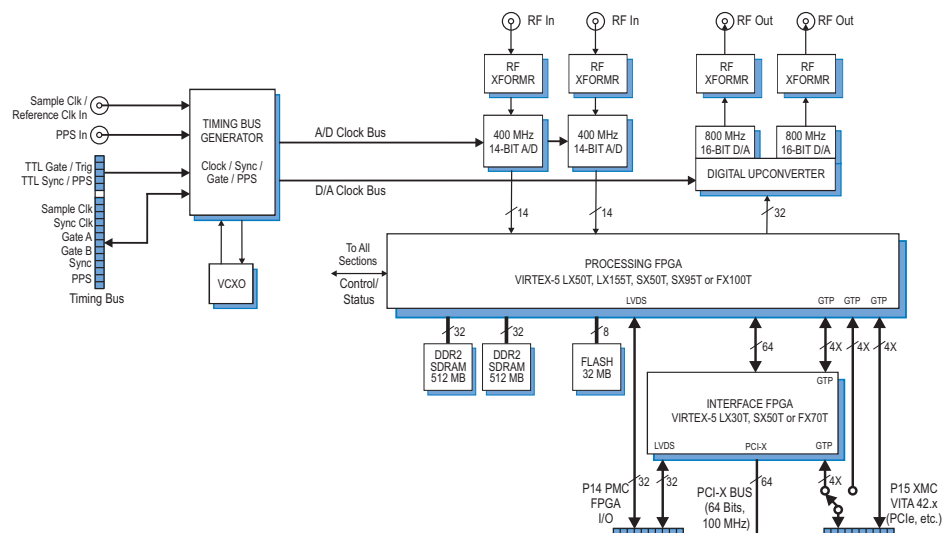
Virtex-5 FPGAs

The Model 7156 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface



XMC Interface

The Model 7156 complies with the VITA 42.0 XMC specification for carrier boards. This standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7156 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 adds the P14 PMC connector with 16 pairs of LVDS connections to each FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 7156's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

PCI-X Interface

The Model 7156 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled,

front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 400 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs the P14 connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA mapped as two 16-bit read/write registers

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7156	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC

Options:

-104	FPGA I/O through the P14 connector
-5xx	XMC interface

Contact Pentek for additional available options.

New!

Model 7158

Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC



Features

- Complete software radio interface solution
- Two 500 MHz, 12-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O on P14

General Information

Model 7158 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters, two Virtex-5 FPGAs and two banks of DDR2 SDRAM. The Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5463 12-bit 500 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing, data capture or routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

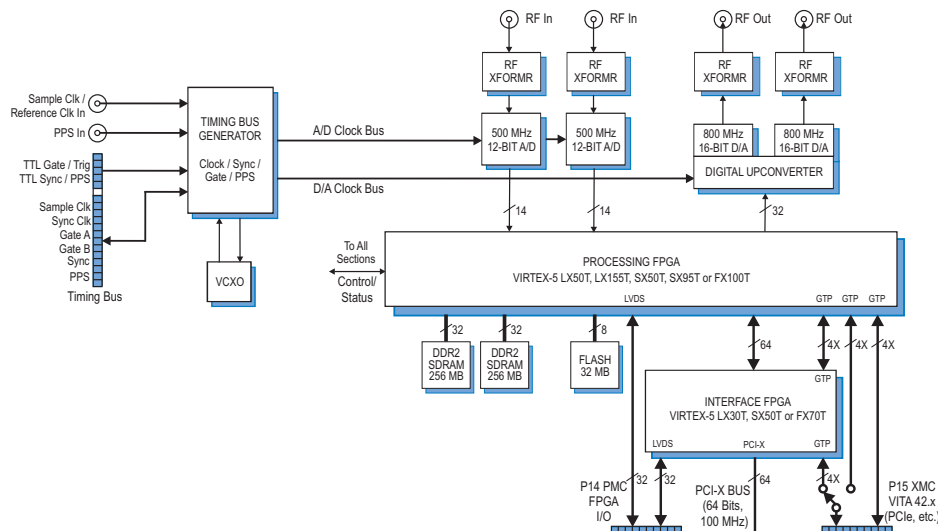
Virtex-5 FPGAs

The Model 7158 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface



XMC Interface

The Model 7158 complies with the VITA 42.0 XMC specification for carrier boards. This standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7158 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 adds the P14 PMC connector with 16 pairs of LVDS connections to each FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can also be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 7158's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Two independent 256 MB banks of DDR2 SDRAM are available to the processing FPGA. These can be upgraded to 512 MB banks with option -140. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

PCI-X Interface

The Model 7158 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 500 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs the P14 connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA mapped as two 16-bit read/write registers

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7158	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC
Options:	
-104	FPGA I/O through the P14 connector
-140	1 GB DDR2 SDRAM
-5xx	XMC interface

Contact Pentek for additional available options.

New!



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User-configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71620 is the first member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchro-

nization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

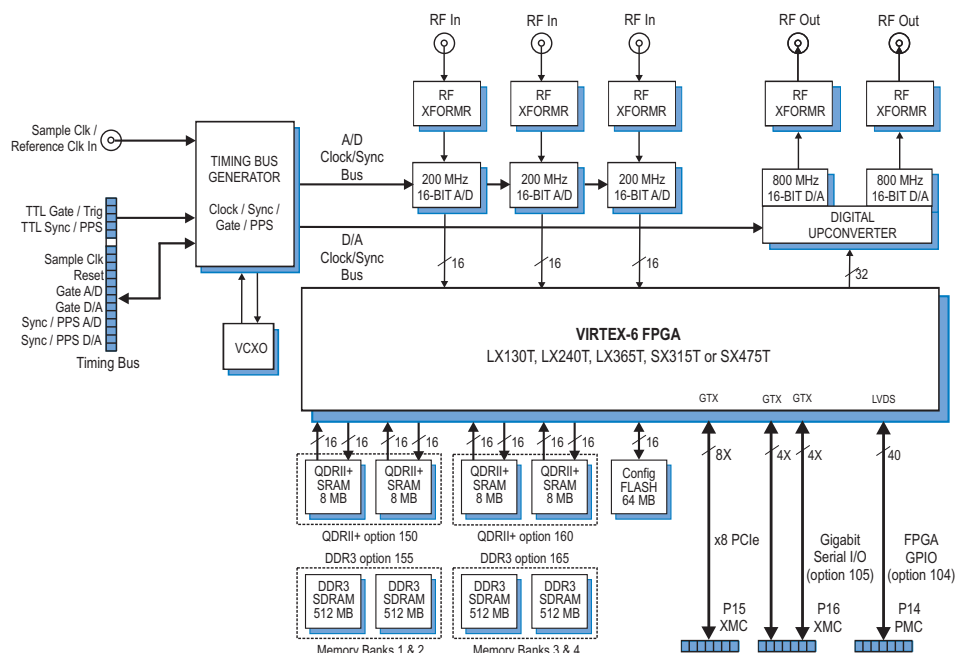
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤



A/D Acquisition IP Modules

The 71620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

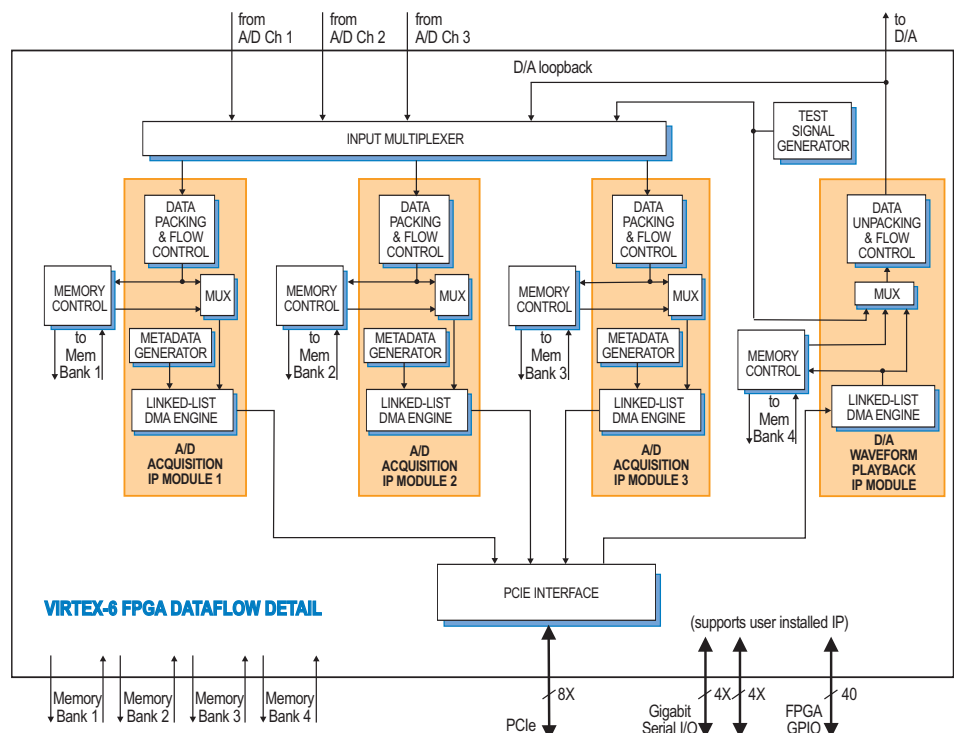
A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



► module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71620 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71620 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Virtex-6

XC6VLX130T

Optional: Xilinx Virtex-6

XC6VLX240T, XC6VLX365T,

XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71620 3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 71621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71621 is a member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71621 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

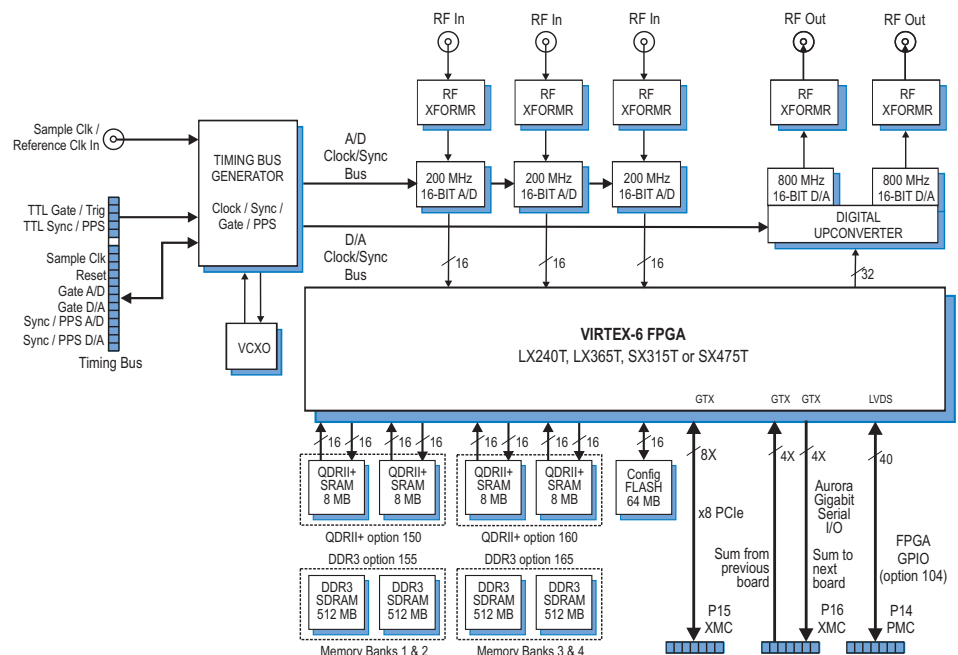
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤



A/D Acquisition IP Modules

The 71621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to

f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Beamformer IP Core

In addition to the DDCs, the 71621 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average

power level of any DDC core falls below or exceeds a programmable threshold.

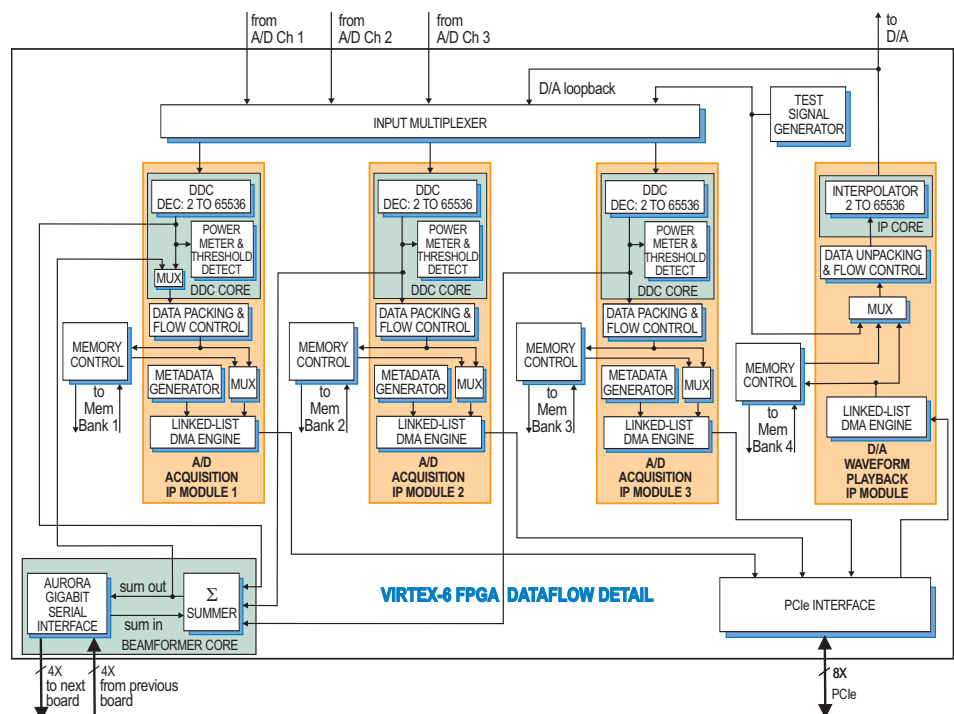
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 71621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TIDAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71621 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71621 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beamforming across multiple boards.

PCI Express Interface

The Model 71621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module. ➤

► Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Digital Downconverters

Quantity: Three channels

Decimation Range: 2 to 65,536 in integer steps

LO Tuning Freq. Resolution: 32 bits, 0 to Fs

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 2 Pi radians

FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation

Resolution: 16 bits

Digital Interpolator

Interpolation Range: 2x to 65,536 in integer steps

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or a 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen.2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71621 3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 71630

1 GHz A/D and D/A, Virtex-6 FPGA - XMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71630 is a member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71630 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 71630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking

and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

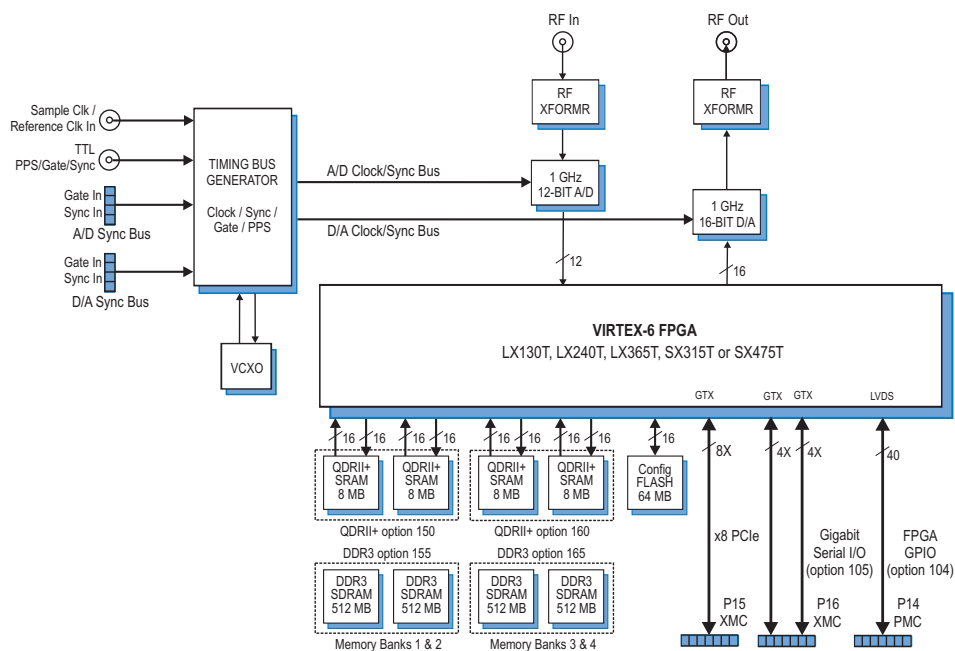
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. ➤



A/D Acquisition IP Module

The 71630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

► A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 71630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to pro-

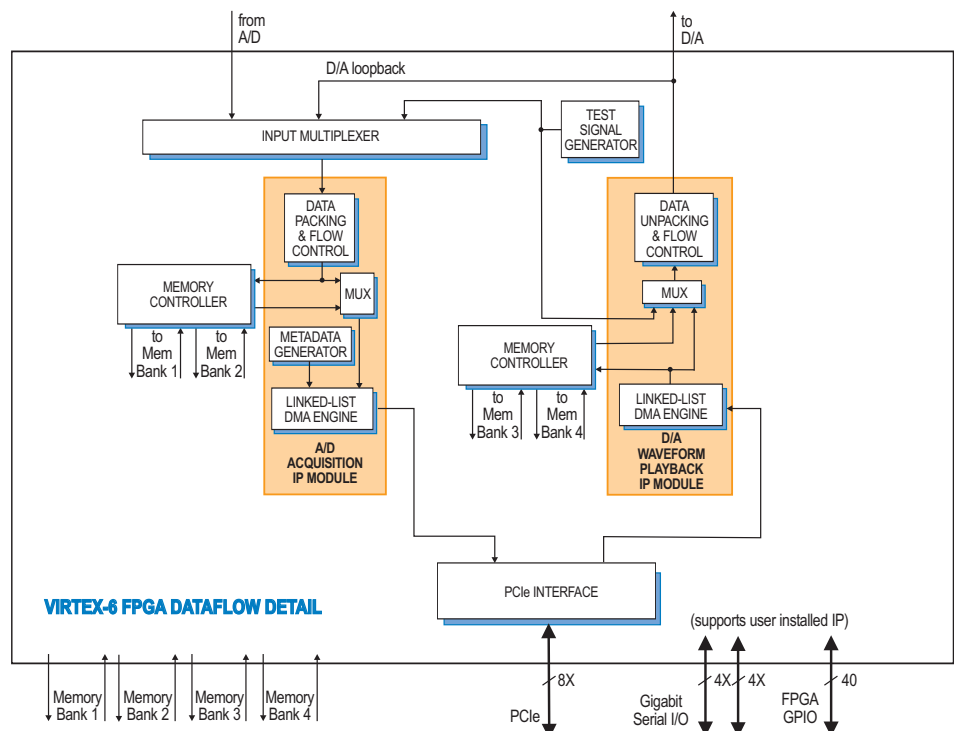
vide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Two front panel 7-pin LVPECL Sync connectors allows multiple modules to be synchronized. One connector for the A/D and one for the D/A each provide sync and gate signals.

Memory Resources

The 71630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ►



► XMC Interface

The Model 71630 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71620 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts sample clock or a 5 or 10 MHz system reference

Timing Bus: 7-pin connectors, LVPECL bus for sync and gate, one A/D connector and one D/A connector

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71630 1 GHz A/D and D/A,
Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 71650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - XMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 2) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71650 is a member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71650 includes optional general-purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 71650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+

memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

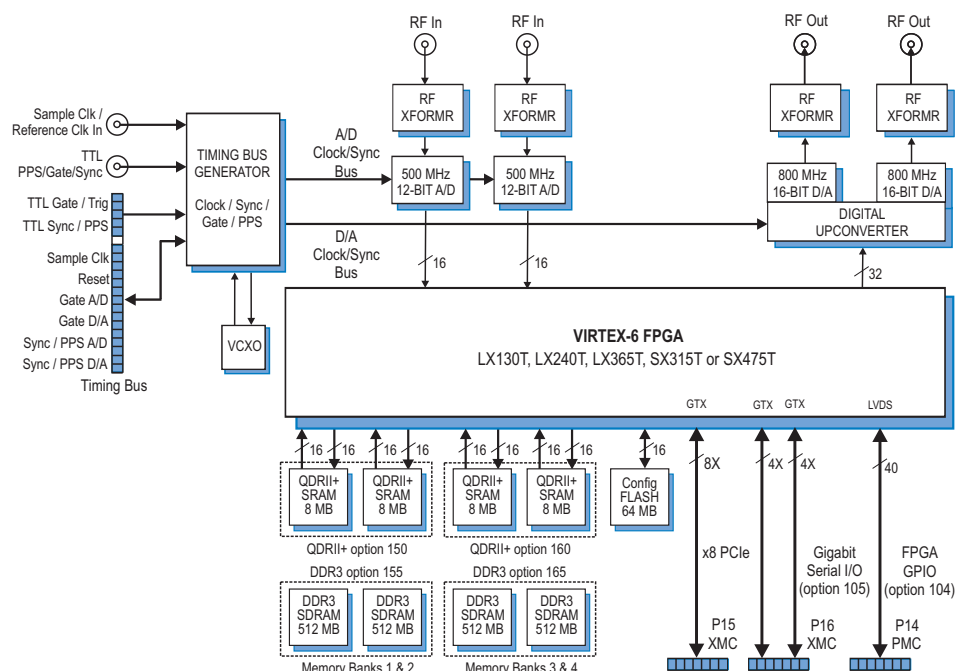
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. ➤



A/D Acquisition IP Modules

The 71650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

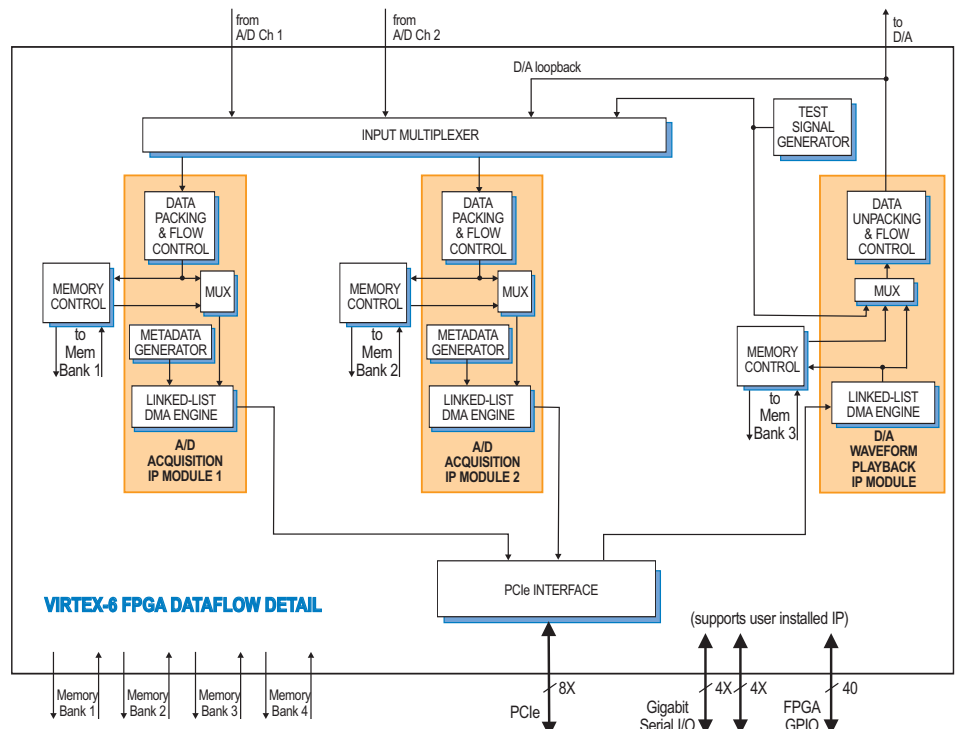
A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 71650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



► module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71650 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71650 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option 014)

Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

D/A Converters

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz, max.
Output IF: DC to 400 MHz, max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz, max. with interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 800 MHz sample clock or a 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs the XMC P16 connector with two 4X serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71650 Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As with Virtex-6 FPGA - XMC

Options:

-014 400 MHz, 14-bit A/Ds
-062 XC6VLX240T
-063 XC6VLX365T
-064 XC6VSX315T
-065 XC6VSX475T
-104 LVDS FPGA I/O through P14 connector
-105 Gigabit serial FPGA I/O through P16 connector
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 71660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - XMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- User-configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71660 is the second member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal

generator, and a PCIe interface complete the factory-installed functions and enable the 71660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

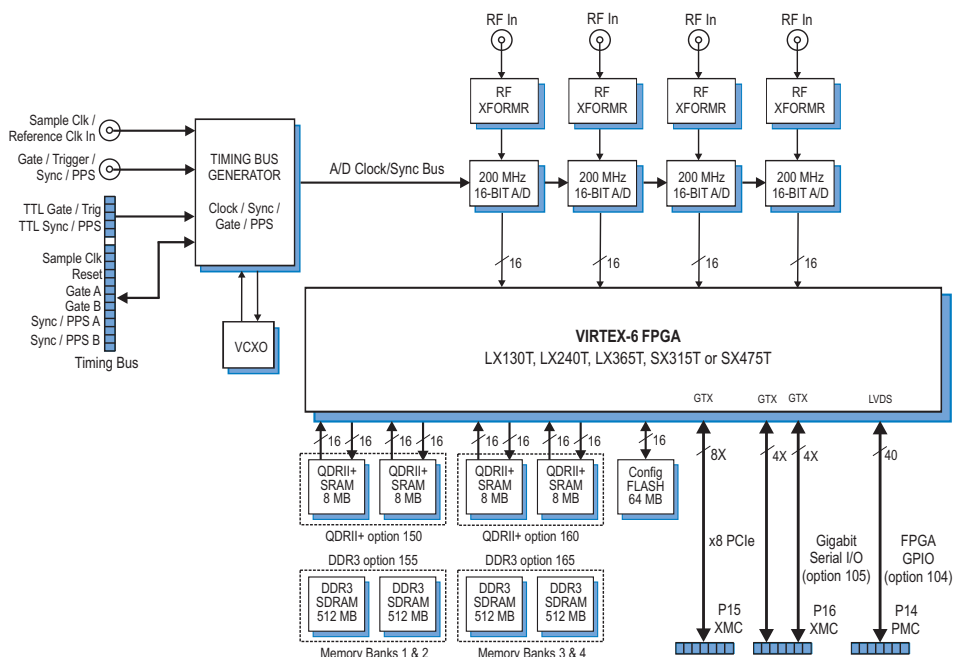
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤



► A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

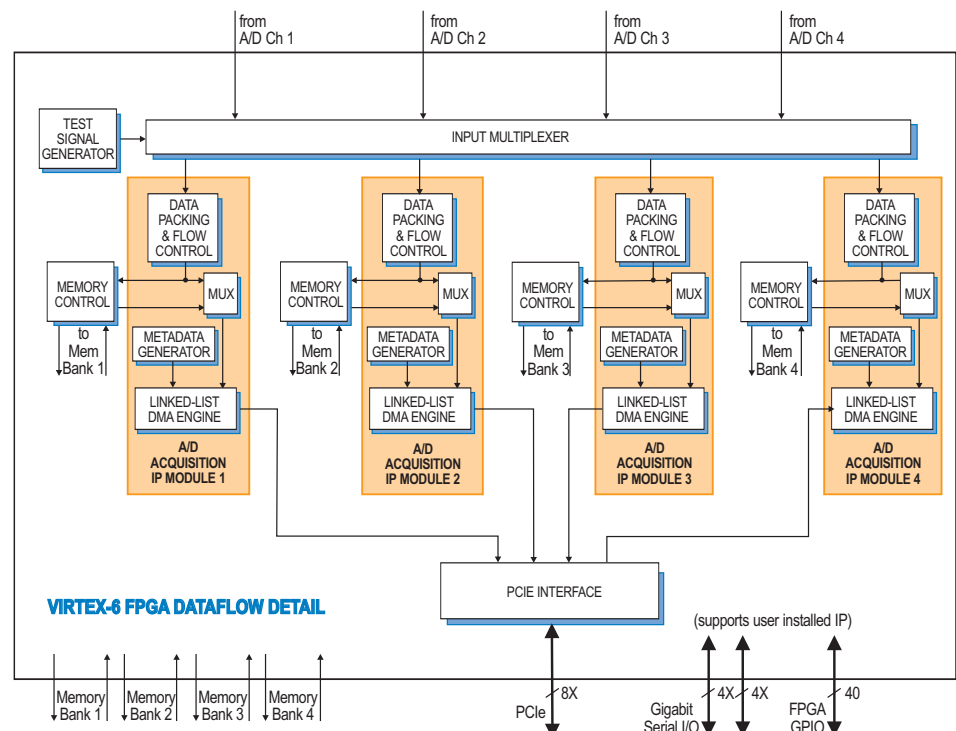
The Model 71660 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71660 ►

A/D Acquisition IP Modules

The 71660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71660 4-Channel 200 MHz A/D with Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 71661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - XMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71661 is a member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71661 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 71661 factory installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules

for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

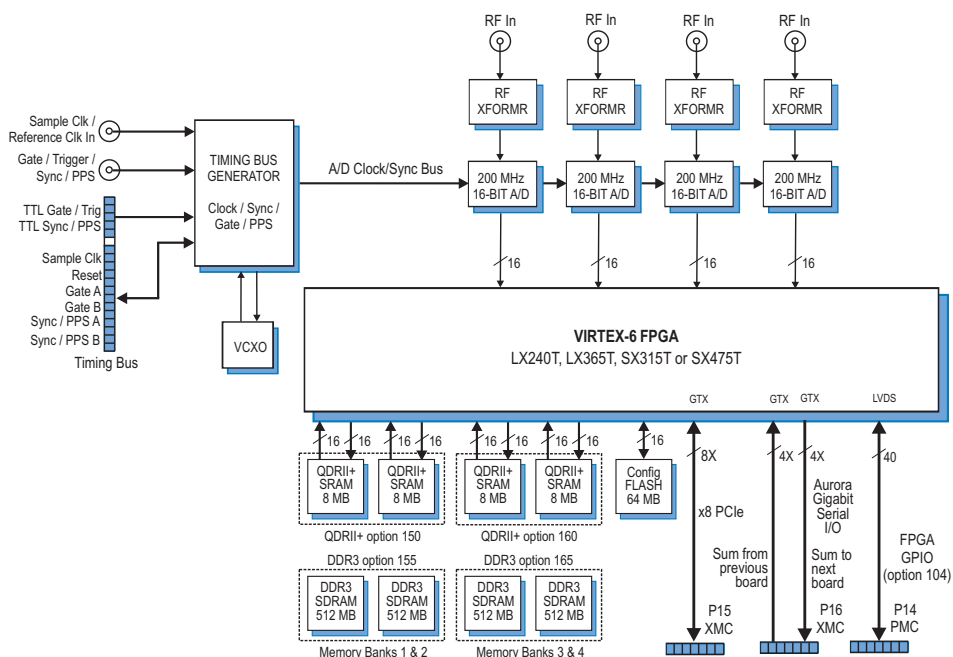
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤



A/D Acquisition IP Modules

The 71661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536

providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Beamformer IP Core

In addition to the DDCs, the 71661 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation

change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

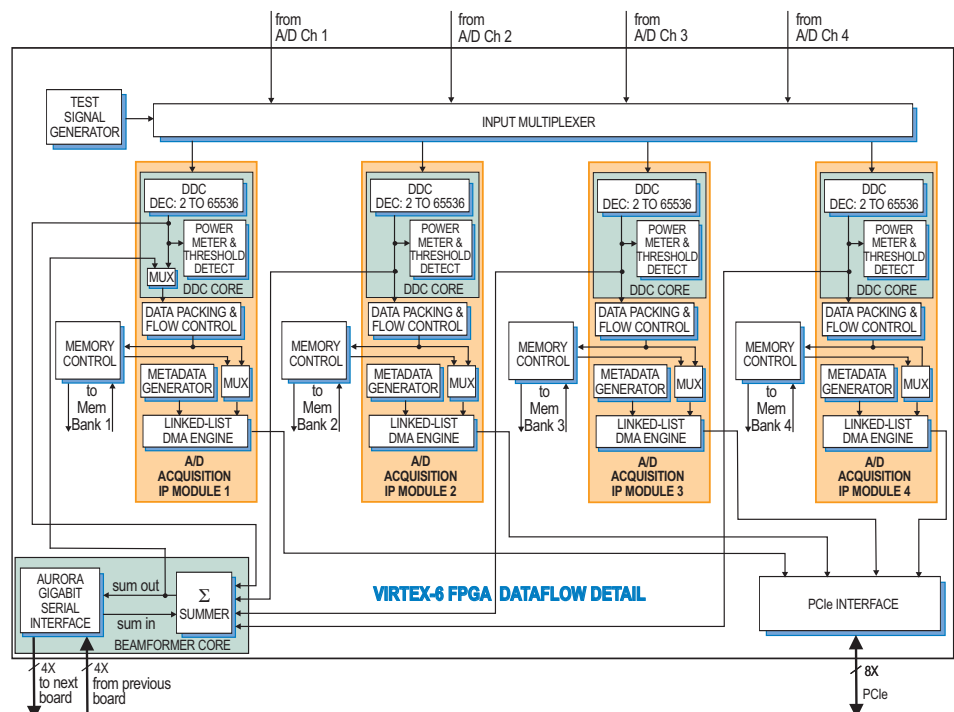
► A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage ►



► controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71661's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71621 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71621 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beam-forming across multiple boards.

PCI Express Interface

The Model 71661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Digital Down converters

Quantity: Four channels

Decimation Range: 2 to 65,536 in integer steps

LO Tuning Freq. Resolution: 32 bits, 0 to Fs

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 2 Pi radians

FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms,

Function: 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen.2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71621 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

RADAR & SDR I/O - CompactPCI

MODEL	DESCRIPTION
7231, 7331	16- or 32-Channel Multiband Receivers with A/Ds and FPGAs - 6U/3U cPCI
7240, 7340	Dual/Quad Multiband Transceivers with FPGAs - 6U/3U cPCI
7240-420, 7340-420	Transceivers with Dual/Quad Wideband DDCs and Interpolation Filters - 6U/3U cPCI
7240-430, 7340-430	Transceivers with 256/512-Channel Narrowband DDC - 6U/3U cPCI
7241, 7341	Dual/Quad Multiband Transceivers with FPGAs - 6U/3U cPCI
7241-420, 7341-420	Transceivers with Dual/Quad Wideband DDCs and Interpolation Filters - 6U/3U cPCI
7241-430, 7341-430	Transceivers with 256/512-Channel Narrowband DDC - 6U/3U cPCI
7242, 7342	Multichannel Transceivers with Virtex-4 FPGAs - 3U/6U cPCI
7242-428, 7342-428	Transceivers with 4/8 Multiband DDCs and Interpolation Filters - 6U/3U cPCI
7250, 7350	Quad or Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 6U/3U cPCI
7251, 7351	256- or 512-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - 6U/3U cPCI
7252, 7352	32- or 64-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - 6U/3U cPCI
7253, 7353	4/8-Channel DDC, 4/8 200 MHz 16-bit A/Ds, Beamformer - 6U/3U cPCI
7256, 7356	Dual/Quad 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U/3U cPCI
7258, 7358	Dual/Quad 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U/3U cPCI
Customer Information	

[RADAR & SDR I/O - PMC/XMC](#)

[RADAR & SDR I/O - PCI](#)

[RADAR & SDR I/O - x16 PCI Express](#)

[RADAR & SDR I/O - x8 PCI Express](#)

[RADAR & SDR I/O - 3U VPX](#)

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Last updated: November 2010



Model 7331 Model 7231D



Features

- Two or four 80 or 105 MHz, 14-bit A/D converters
- 16 or 32 channels of multiband digital downconverters
- 5 kHz to 10 MHz output bandwidth for $f_s = 100$ MHz
- 250 MHz input bandwidth
- Ideal for IF sampling
- User-configurable Xilinx Virtex-II FPGAs
- Custom FPGA I/O through cPCI J2 or J3 and J5 connectors
- Bypass path allows direct capture of A/D data
- Front panel clock and sync bus
- Synchronization of up to 40 7231D or 80 7231 or 7331 with Model 9190

General Information

Models 7231 and 7342 are cPCI multi-channel receivers. They consist of one Model 7131 receiver mounted on a cPCI carrier. The Model 7231 is a 6U cPCI board, while the Model 7331 is a 3U cPCI board. Model 7231D is the same as the Model 7231, except it contains two 7131's rather than one.

Front End

Models 7231 and 7331 accept analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors. Model 7231D accepts up to four analog inputs, while Model 7331 accepts two.

Each input is transformer-coupled and digitized by an AD6645 14-bit A/D converter. The AD6645 operates at a maximum sampling rate of 80 MHz in the standard unit and up to 105 MHz for option -100.

The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, or from an external sample clock supplied through a front panel SMA connector or the front panel sync bus.

Digital Downconverters

These models include four or eight TI/Graychip GC4016 quad multiband downconverter chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable channels capable of center frequency

tuning from DC to $f_s/2$, where f_s is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from two of the A/D converters. A crossbar switch in each GC4016 allows the first 16 channels to select either of the first two A/D outputs, and the second group of 16 downconverter channels (Model 7231D only) to select from the second pair of A/D outputs for flexible switching.

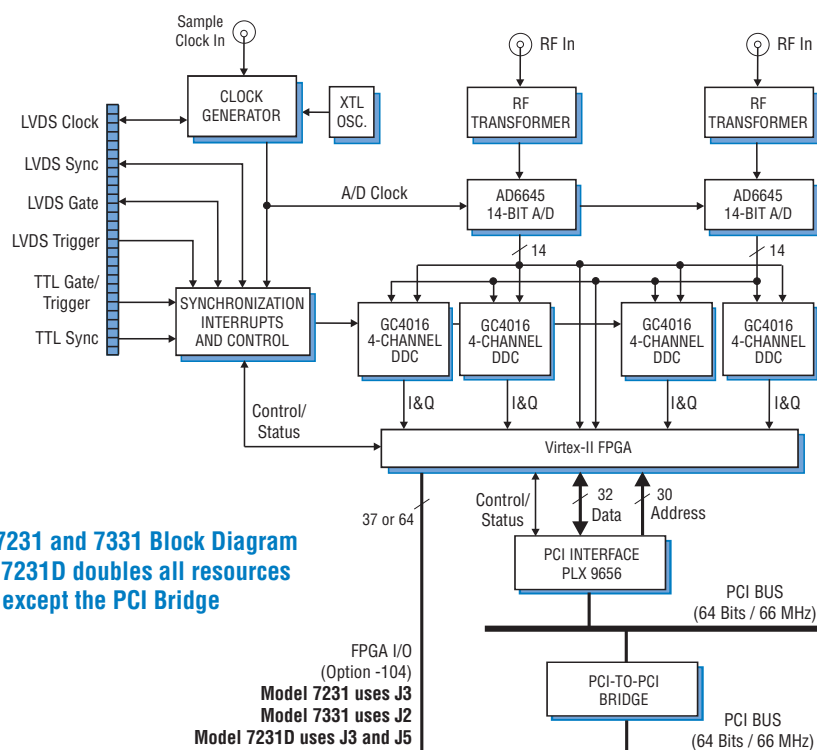
FPGA

The downconverter outputs are delivered to one or two Xilinx Virtex-II XC2V1000 FPGAs with Model 7231, or a single FPGA for Model 7331. Each FPGA is factory configured to perform various modes of data packing, formatting and channel selection, and can be upgraded to an XC2V3000.

Dual port memories in the FPGAs provide efficient PCI bus transfers by buffering downconverter and A/D data.

The A/D outputs are also connected directly to the FPGAs so that wideband A/D data can be delivered directly to the baseboard, bypassing the downconverters.

Option -104 installs the cPCI J3 connector (Model 7231) or the cPCI J2 connector (Model 7331) with 37 signal lines to the XC2V1000 or 64 lines to the XC2V3000 for custom I/O. With Model 7231D, it provides an additional 37 or 64 signal lines to the second FPGA by using the cPCI J5 connector. ➤



Interrupt Sources

These Models have several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload output codes, transitions on the gate signals, clock loss, buffer swapping, or a programmable over-temperature condition or faulty power supply voltage. The ADM1024 Voltage/Temperature Monitor provides constant monitoring of critical voltages and temperatures and generates an interrupt if values exceed threshold limits which are user programmable over the PCI interface.

Ordering Information

Model	Description
7231	16-Channel Multiband Receiver with A/Ds and FPGA - 6U cPCI
7231D	32-Channel Multiband Receiver with A/Ds and FPGAs - 6U cPCI
7331	16-Channel Multiband Receiver with A/Ds and FPFA - 3U cPCI
Options:	
-100	105 MHz A/D with 100 MHz oscillator
-104	FPGA I/O through cPCI J3 for 7231; cPCI J2 for 7331; cPCI J3 and J5 for 7231D
-300	XC2V3000 FPGA replaces XC2V1000

► Output Bandwidth

With a 100 MHz sample clock, the usable output bandwidth of each downconverter channel is 2.5 MHz. However, since these Models deliver parallel digital outputs from the GC4016 into the FPGA(s), users can take advantage of the GC4016 channel combining mode to join two or four channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.

Since each A/D converter connects directly to the FPGA(s), signals with even wider bandwidths can be accommodated.

Synchronization

The front panel clock and sync bus allow one of these Models to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple boards.

Up to four slave 7231D or seven 7231 or 7331 boards can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Using a Pentek Model 9190 Clock and Sync Generator, up to eighty 7331 or 7231 boards or up to forty 7231D boards may be synchronized. In addition to the LVDS timing bus, the Model 7231D can receive up to four TTL front panel input signals: one set of external sync and gate or trigger for the first 16 channels and one set for the second group of 16 channels.

PCI Interface

The FPGA outputs are connected to one (Model 7231 and 7331) or two (Model 7231D) 66 MHz, 64-bit PCI interfaces capable of 528 MB/sec peak data rates. Industry standard PLX9656 PCI interface chips ensure full conformance to all PCI bus timing specifications. A PCI bridge connects the two PCI interfaces to the cPCI backplane for the Model 7231D.

Specifications

Models 7231 and 7331: 16-Channel Configuration

Model 7231D: 32-Channel Configuration Model 7231D shown in the Specifications Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female SMA connectors
Transformer Type: Mini-Circuits ADT4-6T

Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 270 MHz

A/D Converters, Standard (4)

Type: Analog Devices AD6645-80
Sampling Rate: 30 MHz to 80 MHz
Internal Clock: 80 MHz crystal osc.
External Clock: 30 to 80 MHz
Resolution: 14 bits

A/D Converters, Option -100 (4)

Type: Analog Devices AD6645-105
Sampling Rate: 30 MHz to 105 MHz
Internal Clock: 100 MHz crystal osc.
External Clock: 30 to 105 MHz
Resolution: 14 bits

Clock Source (2): Onboard crystal oscillator, front panel ext clock, or LVDS clock

External Clock (2): Front panel female SMA connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms impedance

Sync/Gate Bus (2)

Type: 26-pin connector, with one clock, one sync, and two gate input/output LVDS signals; two trigger LVDS inputs; and one sync and one gate input TTL signals

Digital Downconverters (8)

Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D outputs are connected to all GC4016's
Output: Parallel complex data

Bypass Mode: Data from the A/D converters can be written directly into the FPGAs at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096

Field Programmable Gate Array (2)

Type: Xilinx Virtex-II XC2V1000 standard
Option -300: Virtex-II XC2V3000
Option -104: Installs J3 and J5 connectors with 37 lines to each XC2V1000 or 64 lines to each XC2V3000 FPGA

Dual Port RAM Data Buffers

Quantity: 2 per FPGA
Size: 4k x 32 DPRAM expandable to 8k x 32 with option -300 FPGA

PCI Interface

Type: PLX Technology PCI 9656
PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
Local Bus (FPGA): 32-bit, 66 MHz
Data Transfer Modes: Direct slave mode and DMA mode
PCI Bridge: 64-bit, 66 MHz

Environmental:

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U cPCI board



Model 7340 Model 7240D



Features

- Complete software radio transceiver solution
- Two or four 105 MHz 14-bit A/Ds
- Input signal bandwidth up to 40 MHz
- Four or eight digital downconverters
- One or two digital upconverters
- Two or four 500 MHz 16-bit D/As
- 512 or 1024 MB DDR SDRAM
- One or two Xilinx Virtex-II Pro FPGAs
- Up to 1.28 seconds delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O
- Optional factory-installed IP Cores available

General Information

Models 7240 and 7340 are cPCI multi-band transceivers. They consist of one Model 7140 transceiver mounted on a cPCI carrier. The Model 7240 is a 6U cPCI board, while the Model 7340 is a 3U cPCI board. Model 7240D is the same as the Model 7240, except it contains two 7140's rather than one.

A/D Converter Stage

The front end accepts full scale analog HF or IF inputs on front panel MMCX connectors at +4 dBm into 50 ohms with transformer coupling into AD6645 14-bit 105 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGAs for signal processing or for routing to other board resources.

Digital Downconverter Stages

The TI/Graychip GC4016 quad digital downconverters accept either four 14-bit inputs or three 16-bit digital inputs from the FPGAs, which determine the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the cPCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stages

The TI DAC5686 digital upconverters (DUC) and dual D/As accept baseband real

or complex data streams from the FPGAs with signal bandwidths up to 40 MHz.

When operating as upconverters, they interpolate and translate real or complex baseband input signals to any IF center frequency between DC and 160 MHz. They deliver real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGAs

The Xilinx XC2VP50 Virtex-II Pro FPGAs serve as a control and status engines with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverters, digital upconverters and D/A converters.

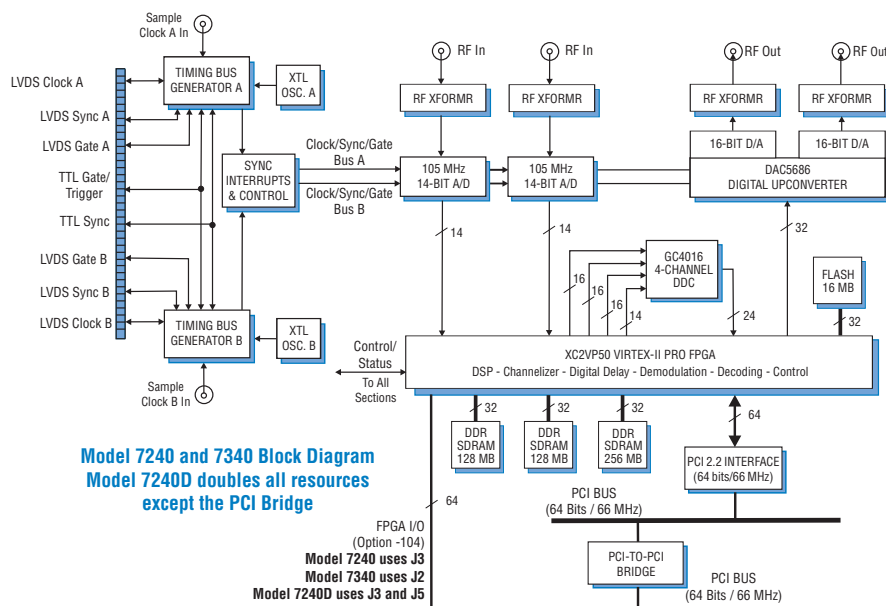
Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Option -104 adds 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O through the cPCI J3 connector. With Model 7240D, the option provides an additional 32 pairs through J5 to the second FPGA.

Each FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals. ➤



► Clocking and Synchronization

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7240D's or seven 7340's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7240 or 7340 boards, or forty 7240D boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

The SDRAMs are also available as a resource for the two PowerPC processor cores within each FPGA. Dual 16 MB FLASH memories support booting and program store for these processors.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7240: Dual Configuration; 7240D: Quad Configuration; 7340: Dual Configuration
7240D shown in the Specifications

Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 270 MHz

A/D Converters (4)

Type: Analog Devices AD6645-105
Sampling Rate: 30 MHz to 105 MHz
Internal Clock: Crystal oscillator A or B
External Clock: 30 to 105 MHz
Resolution: 14 bits

Digital Downconverters (2)

Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
Option -002: -2 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz
Option -002: 400 kHz to 800 MHz

Digital Upconverters (2)

Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel MMCX connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (2)

Type: Xilinx Virtex-II Pro
Option -050: XC2VP50
Option -104: Installs J3 and J5 connectors with 64 lines to each XC2VP50 FPGA

Memory

DDR SDRAM: 1 GB in six banks
FLASH: 32 MB in two banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
Local Bus: 64-bit, 66 MHz
DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U cPCI board

Ordering Information

Model	Description
7240	Dual Multiband Transceiver with FPGA - 6U cPCI
7240D	Quad Multiband Transceiver with FPGA - 6U cPCI
7340	Dual Multiband Transceiver with FPGA - 3U cPCI
Options:	
-002	Full-Scale Output: -2 dBm into 50 ohms; 3 dB Passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through J3 for 7240; J2 for 7340; J3 and J5 for 7240D
-420	GateFlow Installed core: Dual wideband DDC and interpolation filter
-430	GateFlow Installed core: 256-channel narrowband DDC



Model 7340-420

Model 7240D-420



Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz

General Information

Models 7240-420 and 7340-420 are cPCI Transceivers with Dual Wideband DDCs and Interpolation Filters. They consist of one Model 7140-420 transceiver mounted on a cPCI carrier board. Model 7240-420 is a 6U cPCI board, while the Model 7340-420 is a 3U cPCI board. Model 7240D-420 is the same as the Model 7240-420, except it contains two 7140-420's rather than one.

The receiver section features two or four AD6645 105 MHz 14-bit A/D converters and one or two TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, these boards include Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 down-converter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

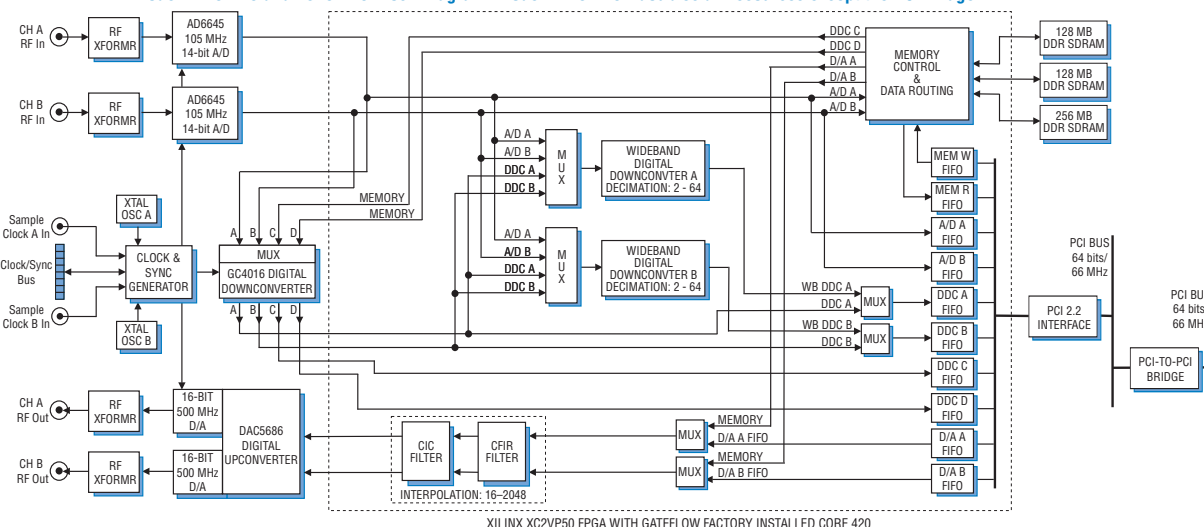
A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of these Models are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤

Model 7240-420 and 7340-420 Block Diagram Model 7240-420D doubles all resources except the PCI Bridge



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7240D-420's or seven 7240-420's or 7340-420's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7240-420 or 7340-420 boards, or forty 7240D-420 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7240-420: Dual Configuration; 7240D-420: Quad Configuration; 7340-420: Dual Configuration

7240D-420 shown in the Specifications Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 270 MHz

A/D Converters (4)

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 30 to 105 MHz

Resolution: 14 bits

Digital Downconverters (2)

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel MMCX connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (2)

Type: Xilinx XC2VP50 Virtex-II Pro

Memory

DDR SDRAM: 1 GB in six banks

FLASH: 32 MB in two banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7240-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - 6U cPCI
7240D-420	GateFlow Transceiver with four Wideband DDCs and two Interpolation Filters factory-installed - 6U cPCI
7340	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - 3U cPCI

Contact Pentek for available options



Model 7340-430

Model 7240D-430



Features

- Complete software radio transceiver solution
- GateFlow Core 430 with 256 or 512 channels of narrowband digital downconverters factory-installed
- 256 or 512 programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

General Information

Models 7240-430 and 7340-430 are cPCI transceivers with 256 channels of narrowband DDCs. They consist of one Model 7140-430 transceiver mounted on a cPCI carrier board. Model 7240-430 is a 6U cPCI board, while the Model 7340-430 is a 3U cPCI board. Model 7240D-430 is the same as the Model 7240-430, except it contains two 7140-430's and doubles the number of channels to 512.

The receiver section features two or four AD6645 105 MHz 14-bit A/D converters and one or two Texas Instruments GC4016 quad multiband digital downconverters. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7140-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC

filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

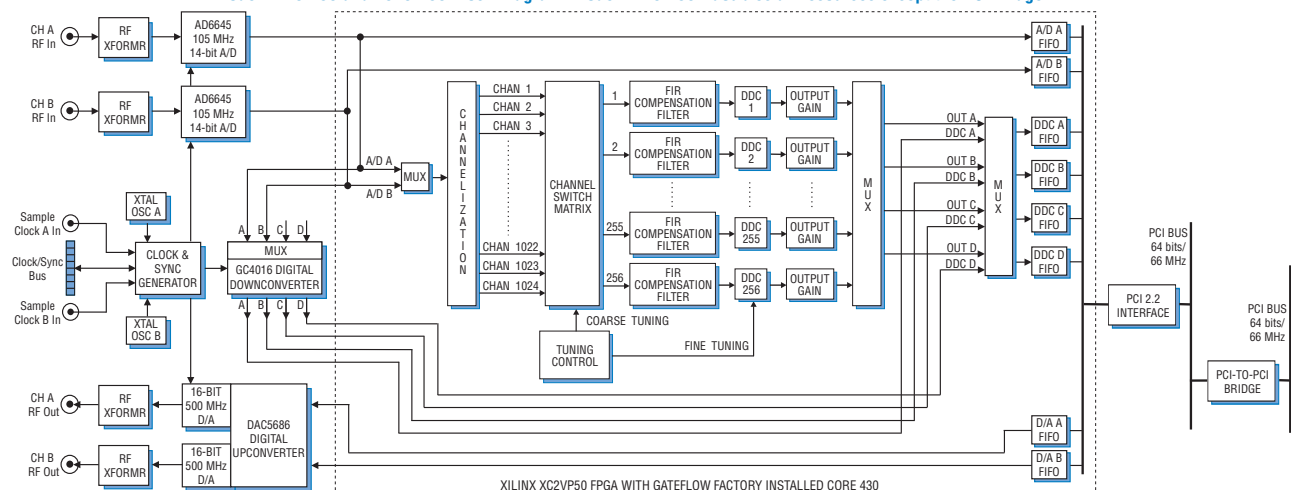
Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2 ³²
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in these Models. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 40 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤

Model 7240-430 and 7340-430 Block Diagram Model 7240-430D doubles all resources except the PCI Bridge



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7240D-430's, or seven slave 7240-430's or 7340-430's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7240-430 or 7340-430 boards, or forty 7240D-430 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7240-430: 256-Channel DDC;
7240D-430: 512-Channel DDC;
7340-430: 256-Channel DDC;
7240D-430 shown in the Specifications

Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 270 MHz

A/D Converters (4)

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 30 to 105 MHz

Resolution: 14 bits

Digital Downconverters (2)

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel MMCX connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (2)

Type: Xilinx XC2VP50 Virtex-II Pro

Memory

DDR SDRAM: 1 GB in six banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7240-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 6U cPCI
7240D-430	GateFlow Transceiver with 512-Channel Narrowband DDC factory-installed - 6U cPCI
7340-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 3U cPCI

Contact Pentek for available options



Model 7341 Model 7241D



Features

- Two or four 125 MHz 14-bit A/Ds
- Input signal bandwidth up to 50 MHz
- Four or eight digital downconverters
- One or two digital upconverters
- Two or four 500 MHz 16-bit D/As
- 512 or 1024 MB DDR SDRAM
- One or two Xilinx Virtex-II Pro FPGAs
- Up to 1.28 seconds delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O
- Optional factory-installed IP Cores available

General Information

Models 7241 and 7341 are cPCI multiband transceivers. They consist of one Model 7141 transceiver mounted on a cPCI carrier. The Model 7241 is a 6U cPCI board, while the Model 7341 is a 3U cPCI board. Model 7241D is the same as the Model 7241, except it contains two 7141's rather than one.

A/D Converter Stage

The front end accepts full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGAs for signal processing or for routing to other board resources.

Digital Downconverter Stages

The TI/Graychip GC4016 quad digital downconverters accept either four 14-bit inputs or three 16-bit digital inputs from the FPGAs, which determine the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the cPCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stages

The TI DAC5686 digital upconverters (DUC) and dual D/As accept baseband real

or complex data streams from the FPGAs with signal bandwidths up to 40 MHz.

When operating as upconverters, they interpolate and translate real or complex baseband input signals to any IF center frequency between DC and 160 MHz. They deliver real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGAs

The Xilinx XC2VP50 Virtex-II Pro FPGAs serve as a control and status engines with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverters, digital upconverters and D/A converters.

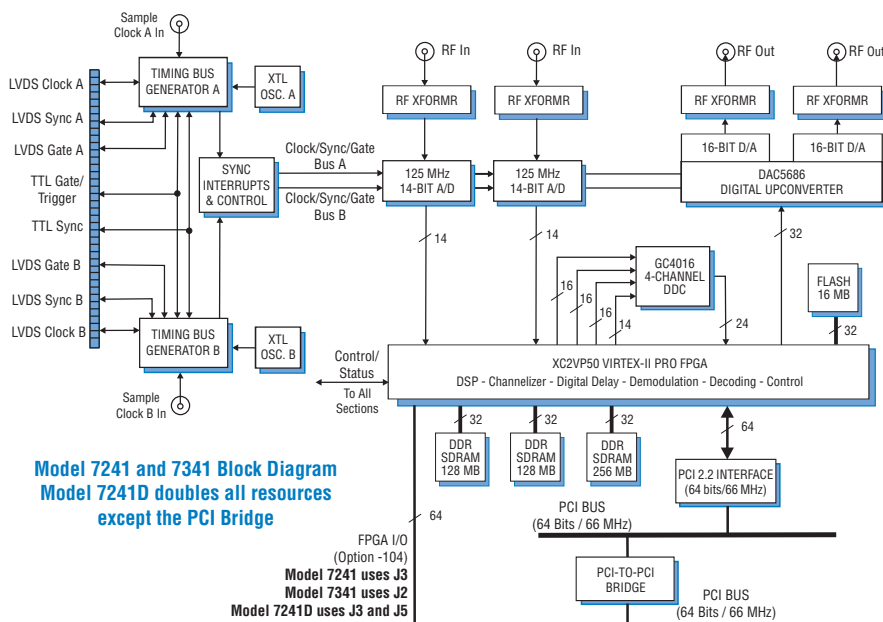
Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Option -104 adds 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O through the cPCI J3 connector. With Model 7241D, the option provides an additional 32 pairs through J5 to the second FPGA.

Each FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals. ➤



► Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7241D's or seven 7341's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7241 or 7341 boards, or forty 7241D boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

The SDRAMs are also available as a resource for the two PowerPC processor cores within each FPGA. Dual 16 MB FLASH memories support booting and program store for these processors.

PCI Interface

These models include an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7241: Dual Configuration

7241D: Quad Configuration

7341: Dual Configuration

7241D shown in the Specifications

Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters (4)

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverters (2)

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

Option -002: -2 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Option -002: 400 kHz to 800 MHz

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (2)

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -104: Installs J3 and J5 connectors with 64 lines to each XC2VP50 FPGA

Memory

DDR SDRAM: 1 GB in six banks

FLASH: 32 MB in two banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7241	Dual Multiband Transceiver with FPGA - 6U cPCI
7241D	Quad Multiband Transceiver with FPGAs - 6U cPCI
7341	Dual Multiband Transceiver with FPGA - 3U cPCI
Options:	
-002	Full-Scale Output: -2 dBm into 50 ohms; 3 dB Passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through J3 for 7241; J2 for 7341; J3 and J5 for 7241D
-125	125 MHz Bus A and 100 MHz Bus B internal oscillators
-420	GateFlow Installed core: Dual wideband DDC and interpolation filter
-430	GateFlow Installed core: 256-channel narrowband DDC



Model 7341-420

Model 7241D-420



Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz

General Information

Models 7241-420 and 7341-420 are cPCI Transceivers with Dual Wideband DDCs and Interpolation Filters. They consist of one Model 7141-420 transceiver mounted on a cPCI carrier board. Model 7241-420 is a 6U cPCI board, while the Model 7341-420 is a 3U cPCI board. Model 7241D-420 is the same as the Model 7241-420, except it contains two 7141-420's rather than one.

The receiver section features two or four LTC2255 125 MHz 14-bit A/D converters and one or two TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, these boards include Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 down-converter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

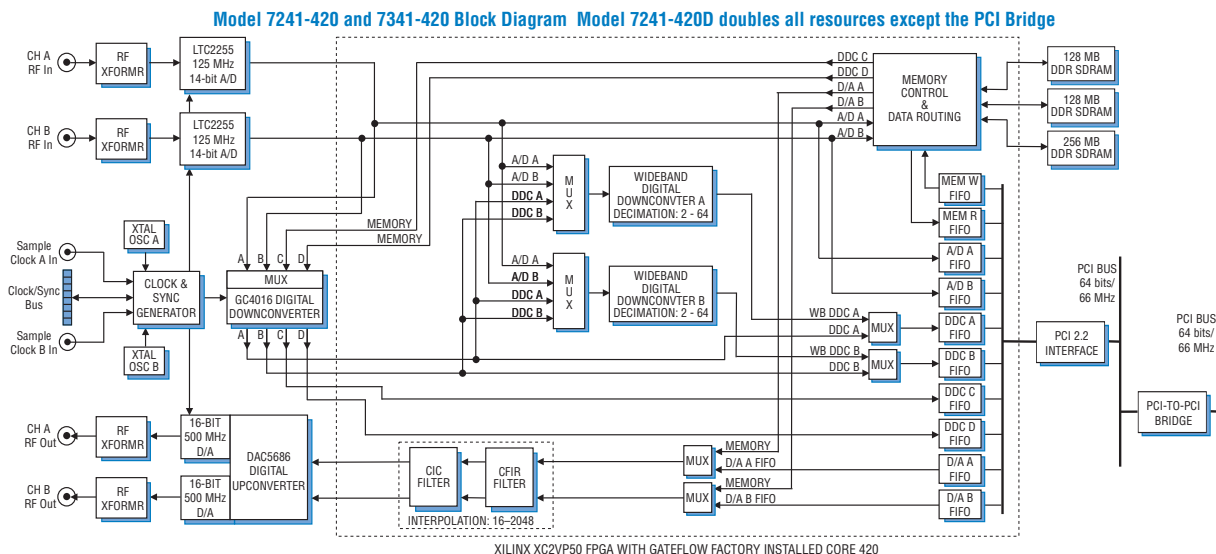
Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of these Models are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤



► **Clocking and Synchronization**

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7241D-420's or seven 7241-420's or 7341-420's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7241-420 or 7341-420 boards, or forty 7241D-420 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7241-420: Dual Configuration; 7241D-420: Quad Configuration; 7341-420: Dual Configuration

7241D-420 shown in the Specifications Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters (4)

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverters (2)

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (2)

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 1 GB in six banks

FLASH: 32 MB in two banks.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7241-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - 6U cPCI
7241D-420	GateFlow Transceiver with four Wideband DDCs and two Interpolation Filters factory-installed - 6U cPCI
7341	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - 3U cPCI

Contact Pentek for available options



Model 7341-430

Model 7241D-430



Features

- Complete software radio transceiver solution
- GateFlow Core 430 with 256 or 512 Channels of Narrowband Digital Downconverters factory-installed
- 256 or 512 programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

General Information

Models 7241-430 and 7341-430 are cPCI transceivers with 256 channels of narrowband DDCs. They consist of one Model 7141-430 transceiver mounted on a cPCI carrier board. Model 7241-430 is a 6U cPCI board, while the Model 7341-430 is a 3U cPCI board. Model 7241D-430 is the same as the Model 7241-430, except it contains two 7141-430's and doubles the number of channels to 512.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7141-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC

filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

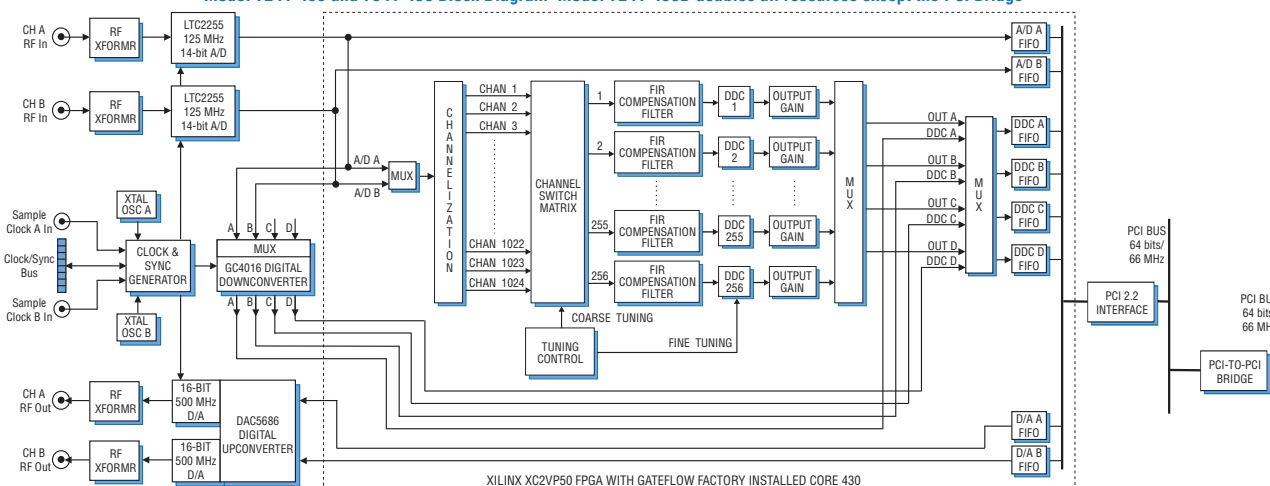
Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2 ³²
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in these Models. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤

Model 7241-430 and 7341-430 Block Diagram Model 7241-430D doubles all resources except the PCI Bridge



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7241-430's or 7341-430's, or four slave 7241D-430's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7241-430 or 7341-430 boards, or forty 7241D-430 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7241-430: 256-Channel DDC; 7241D-430: 512-Channel DDC; 7341-430: 256-Channel DDC

7241D-430 shown in the Specifications

Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters (4)

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverters (2)

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (2)

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 1 GB in six banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7241-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 6U cPCI
7241D-430	GateFlow Transceiver with 512-Channel Narrowband DDC factory-installed - 6U cPCI
7341-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 3U cPCI

Contact Pentek for available options



Model 7342 Model 7242D



Features

- Complete software radio transceiver solution
- Four or eight 125 MHz 14-bit A/Ds
- One or two digital upconverters
- One or two 500 MHz 16-bit D/As
- 768 or 1536 MB DDR2 SDRAM
- Two or four Xilinx Virtex-4 FPGAs
- Up to 2.0 seconds of delay or data capture at 125 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-4 FPGAs for custom I/O
- Optional factory-installed IP Cores available

General Information

Models 7242 and 7342 are cPCI multi-channel transceivers. They consist of one Model 7142 transceiver mounted on a cPCI carrier. The Model 7242 is a 6U cPCI board, while the Model 7342 is a 3U cPCI board. Model 7242D is the same as the Model 7242, except it contains two 7142's rather than one.

A/D Converter Stage

The front end accepts four or eight full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into the Virtex-4 FPGAs for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

One or two TI DAC5686 digital upconverters (DUC) and D/As accept base-band real or complex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as upconverters, they interpolate and translate real or complex baseband input signals to any IF center frequency between DC and 160 MHz. They deliver real or quadrature (I+Q) analog outputs at up to 320 MHz to the 16-bit D/A converters. Analog outputs are through front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686's act as interpolating 16-bit D/As with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

The architecture includes two or four Virtex-4 FPGAs. All of the board's data and

control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can include their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

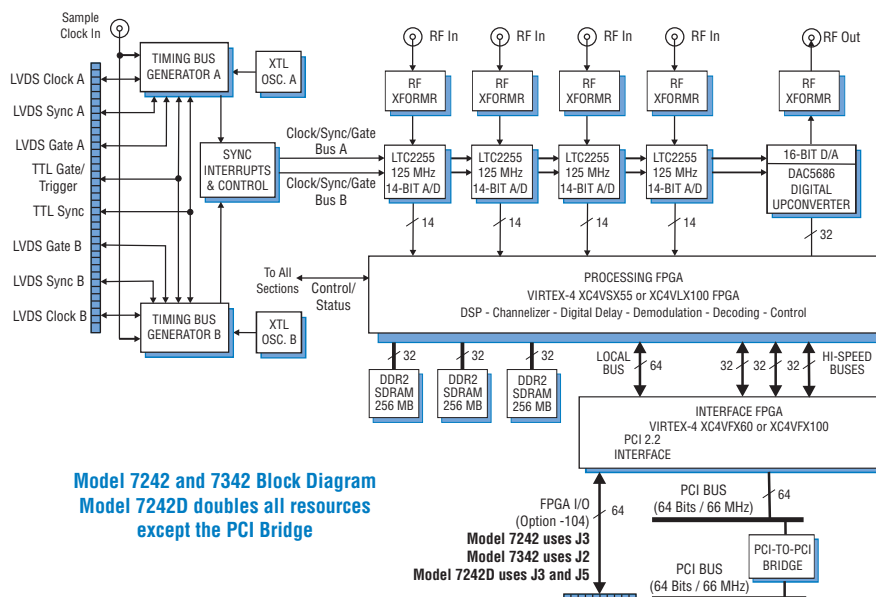
The Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverters and D/A converters.

The XC4VSX55 features 512 DSP slices and is ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission.

For applications requiring more FPGA logic cells, these Models can be optionally configured with an XC4VLX100 in place of the XC2VSX55 for 110,592 logic cells.

A second Virtex-4 FPGA provides board interfaces including PCI and serial I/O. The XC4VFX60 FPGAs also include two PowerPC cores which can be used as local microcontrollers to create complete application engines. These Models can be optionally configured with an XC4VFX100 in place of the XC4VFX60.

Option -104 installs the J3 connector (Model 7242) or the J2 connector (Model 7342) with 32 pairs of LVDS lines to the first XC4VFX60/100 FPGA for custom I/O. With Model 7242D, an additional 32 pairs of LVDS lines connect to the second XC4VFX60/100 FPGA through J5. ➤



Model 7242 and 7342 Block Diagram
Model 7242D doubles all resources except the PCI Bridge

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the upconverters and the D/A. Two internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to four slave 7242's and seven slave 7342's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to forty 7242 boards or eighty 7342 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator. All memory banks can be easily accessed through the PCI interface.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

These Models include an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the board.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Model 7242 or Model 7342: 4 A/D, 1 D/A

Model 7242D: 8 A/D, 2 DUC & 2 D/A

Model 7242D shown in the Specifications Front Panel Analog Signal Inputs (8)

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters (8)

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal osc.

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Outputs (2)

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms (other options available)

3 dB Passband: 60 kHz to 300 MHz (other options available)

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (4)

Type: Two Xilinx Virtex-4 XC4VSX55 & Two Xilinx Virtex-4 XC4VFX60

Option -100: XC4VFX100 replaces XC4VFX60

Option -110: XC4VLX100 replaces XC4VSX55

Custom I/O

Option -104: Installs J3 and J5 connectors with 32 pairs of lines to each XC4VFX60/100 FPGA

Memory

DDR2 SDRAM: 1536 MB in six banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7242	Multichannel Transceiver with Virtex-4 FPGAs - 6U cPCI
7242D	Multichannel Transceiver with Virtex-4 FPGAs - 6U cPCI, with two 7142 modules
7342	Multichannel Transceiver with Virtex-4 FPGAs - 3U cPCI
Options:	
-100	XC4VFX100 replaces XC4VFX60
-104	FPGA I/O through cPCI J3 for 7242; cPCI J2 for 7342; cPCI J3 and J5 for 7242D
-110	XC4VLX100 replaces XC4VSX55
-428	Four multiband DDCs and interpolation filter, factory-installed core



Model 7342-428

Model 7242D-428



Features

- Complete software radio transceiver solution
- GateFlow IP Core 428, with four or eight high-performance multiband DDCs and one or two Interpolation Filters, factory-installed
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4

General Information

Models 7242-428 and 7342-428 are cPCI Transceivers with four or eight Multiband DDCs and one or two Interpolation Filters. They consist of one Model 7142-428 transceiver mounted on a cPCI carrier board. Model 7242-428 is a 6U cPCI board, while the Model 7342-428 is a 3U cPCI board. Model 7242D-428 is the same as the Model 7242-428, except it contains two 7142-428's rather than one.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other module resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The

DDCs consist of two cascaded decimating FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

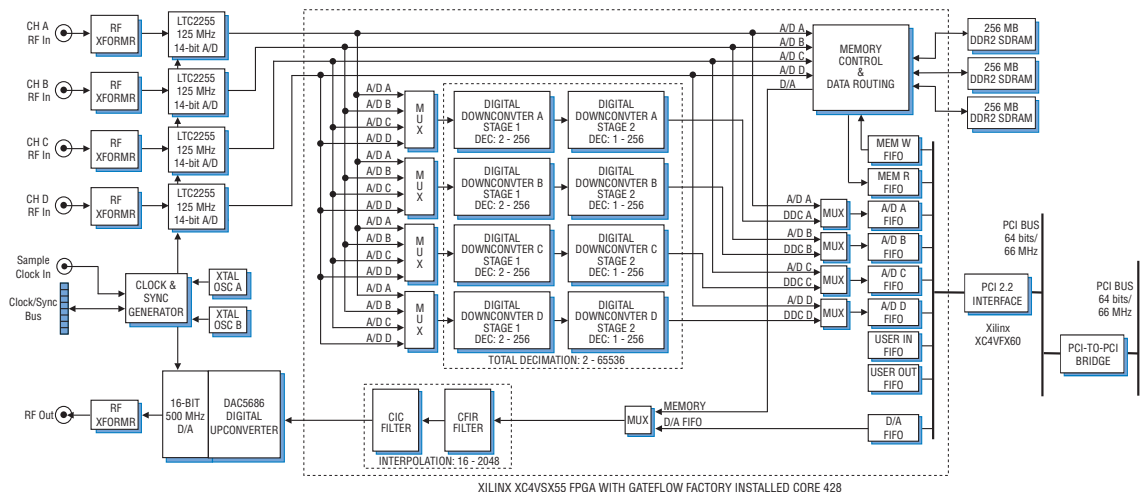
The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ➤

Model 7242-428 and 7342-428 Block Diagram Model 7242-428D doubles all resources except the PCI Bridge



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 7242-428's or 7342-428's, or four 7242D-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7242-428 or 7342-428 boards, or forty 7242D-428 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7242-428: Dual Configuration; 7242D-428: Quad Configuration; 7342-428: Dual Configuration
7242D-428 shown in the Specifications

Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters (4)

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverters (2)

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (4)

Type: Two Xilinx Virtex-4 XC4VSX55 and two Xilinx Virtex-4 XC4VFX60

Memory

DDR SDRAM: 1 GB in six banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7242-428	GateFlow Transceiver with four Multiband DDCs and one Interpolation Filter factory-installed - 6U cPCI
7242D-428	GateFlow Transceiver with eight Multiband DDCs and two Interpolation Filters factory-installed - 6U cPCI
7342-428	GateFlow Transceiver with four Multiband DDCs and one Interpolation 3U cPCI

Contact Pentek for available options

New!

Models 7250, 7250D and 7350

Quad or Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - cPCI



Model 7350 Model 7250D



Features

- Complete software radio interface solutions
- Four or eight 200 MHz, 16-bit A/Ds
- Up to 1.5 or 3.0 GB of DDR2 SDRAM
- Two or four Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Models 7250 and 7350 are cPCI Quad 200 MHz A/Ds. They consist of one Model 7150 Quad A/D mounted on a cPCI carrier. The Model 7250 is a 6U cPCI board, while the Model 7350 is a 3U cPCI board. Model 7250D is the same as the Model 7250, except it contains two 7150's rather than one.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into Xilinx Virtex-5 FPGAs for routing, formatting and DDC signal processing operations.

Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of

different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Models 7250 and 7350 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

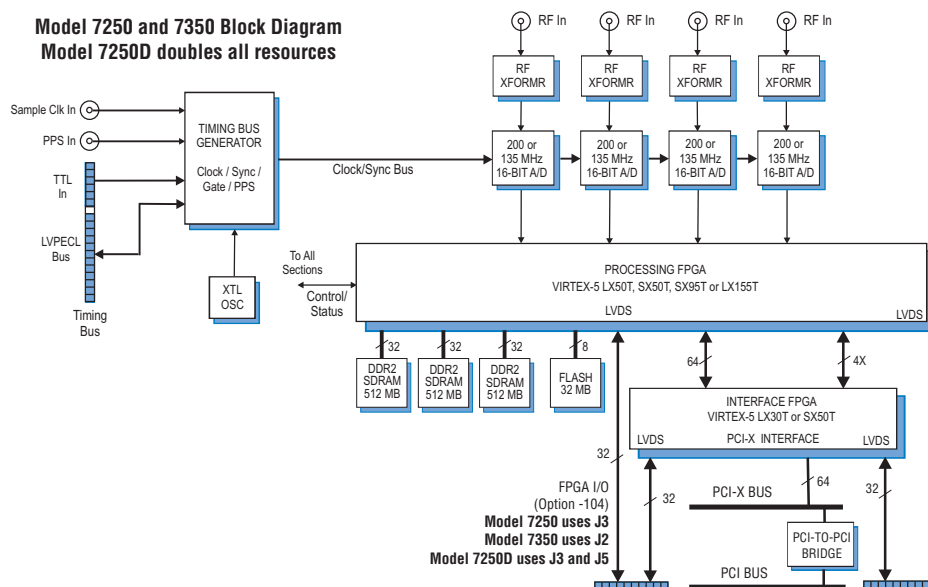
Option -104 installs the J3 connector (Model 7250) or the J2 connector (Model 7350) with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

With Model 7250D, the option provides an additional 16 pairs of LVDS connections through the J5 connector to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ➤

Model 7250 and 7350 Block Diagram
Model 7250D doubles all resources



► Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to two slave 7250Ds and three slave 7350s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

Both Models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33, and 66 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, these Models can be optionally factory-configured with x4 PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Specifications

Model 7250 or Model 7350: 4 A/Ds

Model 7250D: 8 A/Ds

Model 7250D shown in the Specifications Front Panel Analog Signal Inputs (8)

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources (4): Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks (4)

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPSinput/outputLVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array (4)

Processing FPGA: Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XCV5FX100T

Interface FPGA: Two Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs the J3 and J5 cPCI connectors with 32 pairs of LVDS connections to the processing FPGA and 32 pairs of LVDS connections to the interface FPGA for custom I/O

Memory

DDR2 SDRAM: Up to 3.0 GB in six banks

PCI Interface

PCI Bus: 32- or 64-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7250	Quad 200 MHz, 16-bit A/D with two Virtex-5 FPGAs - 6U cPCI
7250D	Octal 200 MHz, 16-bit A/D with four Virtex-5 FPGAs - 6U cPCI
7350	Quad 200 MHz, 16-bit A/D with two Virtex-5 FPGAs - 3U cPCI
Options:	
-104	FPGA I/O through cPCI J3 for 7250 or J2 for 7350; cPCI J3 and J5 for 7250D

Contact Pentek for additional available options.

New!

Models 7251, 7251D and 7351

256 or 512-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - cPCI



Model 7351 Model 7251D

Features

- 256 or 512 channels of DDC
- Four or eight 200 MHz 16-bit A/Ds
- Independent tuning for each channel
- DDC decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization

General Information

Models 7251 and 7351 are high-speed software radio cPCI boards. They consist of one Model 7151 Quad A/D digitizer with a factory-installed high-performance 256-channel DDC IP Core mounted on a cPCI carrier board. The Model 7251 is a 6U cPCI board, while the Model 7351 is a 3U cPCI board. Model 7251D is the same as the Model 7251, except it contains two 7151's rather than one.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into Xilinx Virtex-5 FPGAs for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

These Models employ an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 256 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.



Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 * f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

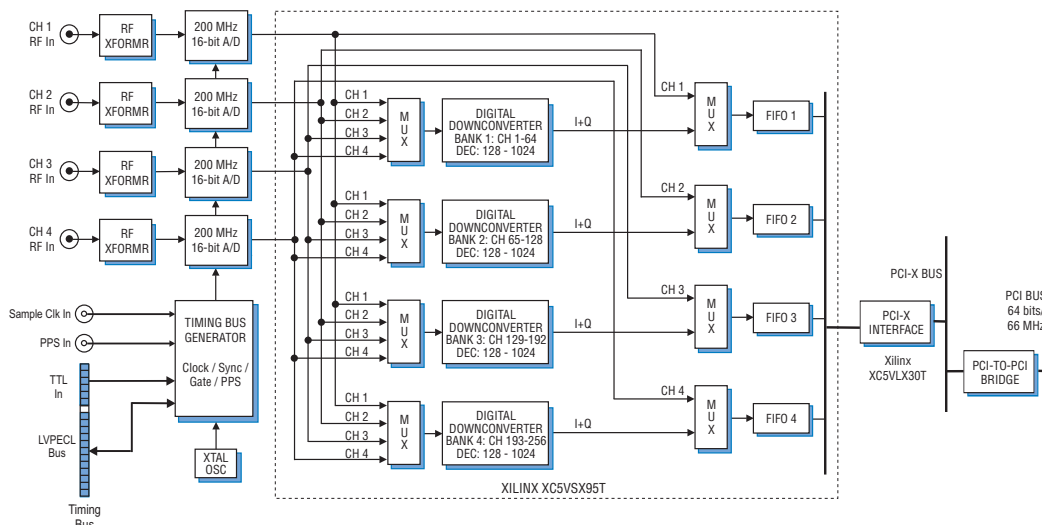
Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wide-band A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus. ➤

Model 7251 and 7351 Block Diagram Model 7251D doubles all resources except the PCI Bridge



► Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to two slave 7251Ds or three slave 7351s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI Interface

Both models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the boards.

Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported.

Specifications

Model 7251 or 7351: 4 A/Ds, 256-channel DDC

Model 7251D: 8 A/Ds, 512-channel DDC
Model 7251D shown in the Specifications

Front Panel Analog Signal Inputs (8)

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources (4): Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks (4)

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array (4)

Processing FPGA: Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface

PCI Bus: 32 or 64 bits at 66 MHz and 32 or 64 bits at 33 MHz

DMA: 8 channel demand-mode and chaining controller

Local Bus: 64 bits at 33, 66 and 100 MHz

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: standard 6U cPCI board

Ordering Information

Model	Description
7251	256-Channel DDC with four 200 MHz, 16-bit A/Ds - 6U cPCI
7251D	512-Channel DDC with eight 200 MHz, 16-bit A/Ds - 6U cPCI
7351	256-Channel DDC with four 200 MHz, 16-bit A/Ds - 3U cPCI

Options:

-730	Two-slot heat sink

Contact Pentek for available options.

New!

Models 7252, 7252D and 7352

32 or 64-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - cPCI



Model 7352 Model 7252D

Features

- 32 or 64-channel DDC with four or eight banks of 8 channels
- Four or eight 200 MHz, 16-bit A/Ds
- Independent 32-bit DDC tuning for all channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths: 20 kHz to 10 MHz
- Different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multiboard synchronization

General Information

Models 7252 and 7352 are high-speed software radio cPCI boards. They consist of one Model 7152 Quad A/D digitizer with a factory-installed high-performance 32-channel DDC IP Core mounted on a cPCI carrier board. The Model 7252 is a 6U cPCI board, while the Model 7352 is a 3U cPCI board. Model 7252D is the same as the Model 7252, except it contains two 7152's rather than one.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into Xilinx Virtex-5 FPGAs for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

These Models employ an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 32 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

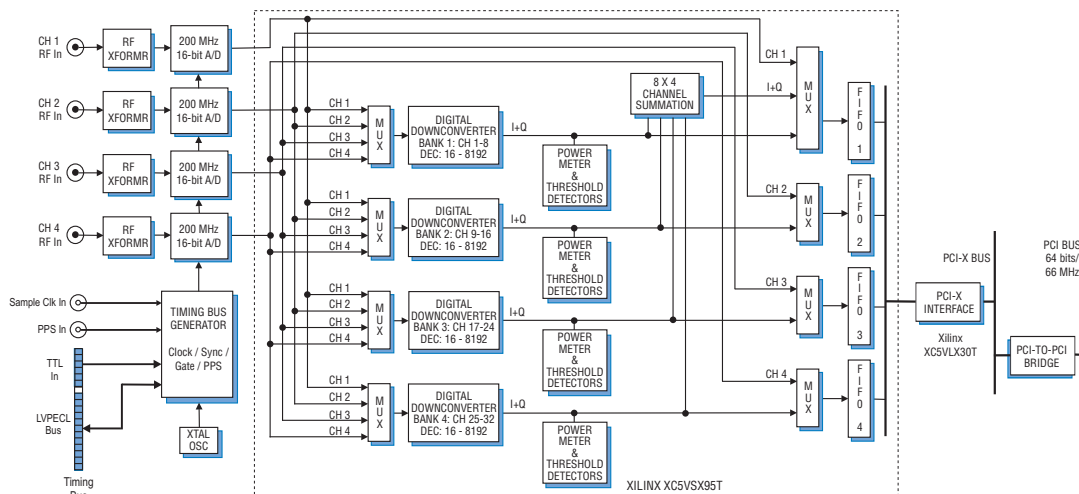
Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

These models feature 32 power meters that continuously measure the individual average power output of each of the 32 DDC channels. The time constant of the averaging interval for each meter is programmable up to 16K samples. In addition, 32 threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤



Model 7252 and 7352 Block Diagram Model 7252D doubles all resources except the PCI Bridge



► Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to two slave 7252Ds or three slave 7352s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI Interface

Both models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the boards.

Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported.

Ordering Information

Model	Description
7252	32-Channel DDC with four 200 MHz, 16-bit A/Ds - 6U cPCI
7252D	64-Channel DDC with eight 200 MHz, 16-bit A/Ds - 6U cPCI
7352	32-Channel DDC with four 200 MHz, 16-bit A/Ds - 3U cPCI

Options:

-730	Two-slot heat sink

Contact Pentek for available options.

Specifications

Model 7252 or 7352: 4 A/Ds, 32-channel DDC

Model 7252D: 8 A/Ds, 64-channel DDC

Model 7252D shown in the Specifications
Front Panel Analog Signal Inputs (8)

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources (4): Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks (4)

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array (4)

Processing FPGA: Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface

PCI Bus: 32 or 64 bits at 66 MHz and 32 or 64 bits at 33 MHz

DMA: 8 channel demand-mode and chaining controller

Local Bus: 64 bits at 33, 66 and 100 MHz

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

New!

Models 7253, 7253D and 7353

4/8-Ch. DDC, 4/8 200 MHz 16-bit A/Ds, Beamformer - cPCI



Model 7353 Model 7253D

Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- 6U and 3U cPCI boards
- 2 or 4 (Models 7253 and 7353) and 4 or 8 (Model 7253D) channels of DDC
- Four or eight 200 MHz, 16-bit A/Ds
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- LVPECL clock/sync bus for multiboard synchronization

General Information

Models 7253 and 7353 are high-speed software radio boards designed for processing baseband RF or IF signals from a communications receiver. They feature four 200 MHz 16-bit A/Ds (Models 7253 and 7353) or eight A/Ds (Model 7253D). Each group of four A/Ds is supported by a high-performance 4-channel installed DDC and a complete set of beamforming functions. With built-in multiboard synchronization, they are ideally matched to the requirements of real-time software radio and radar systems.

Model 7253 is a 6U cPCI board while Model 7353 is a 3U cPCI board. Model 7253D is the same as the 7253 except it provides twice the resources.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into Xilinx Virtex-5 FPGAs for routing, formatting and signal processing.

DDC Input Selection and Tuning

These Models employ an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be

achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency.

Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

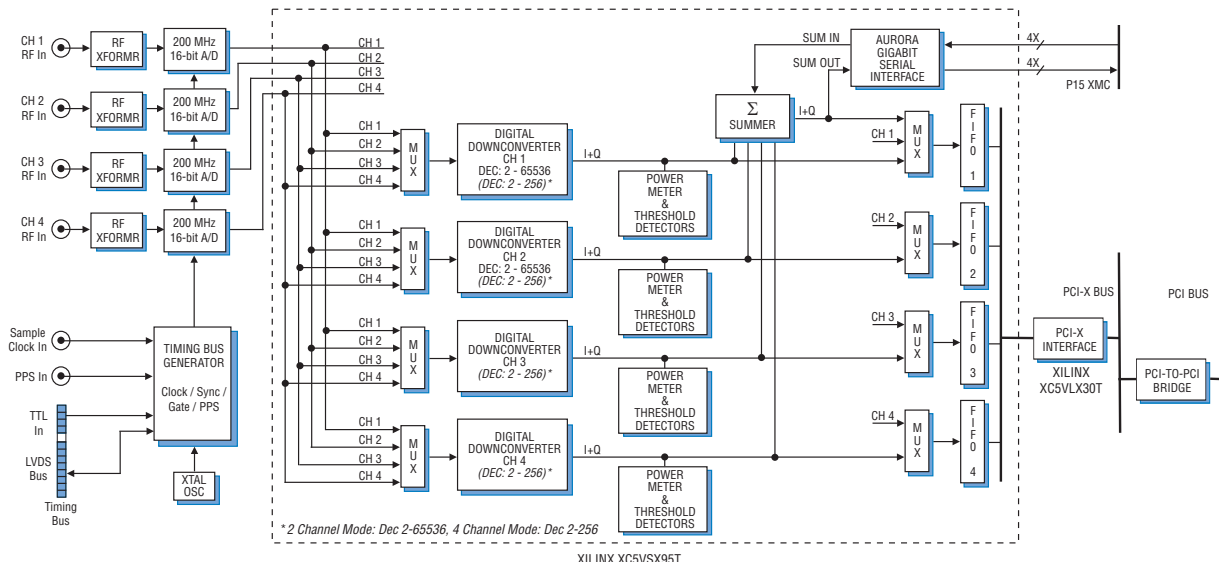
The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N .

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the ➤



Model 7253 and 7353 Block Diagram Model 7253D doubles all resources except the PCI Bridge



XMC Interface

For large systems, multiple 7253's, 7353's or 7253Ds can be chained together via a built-in Xilinx Aurora interface through the P15 XMC connector.

This link creates a board-to-board summation expansion chain for creating larger multi-channel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

► calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications.

Beamformer

In addition to the A/Ds and DDCs, these Models include essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable-gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCI bus.

For larger systems, multiple Models can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates an x4 sum output stream to the next board through the P15 XMC connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

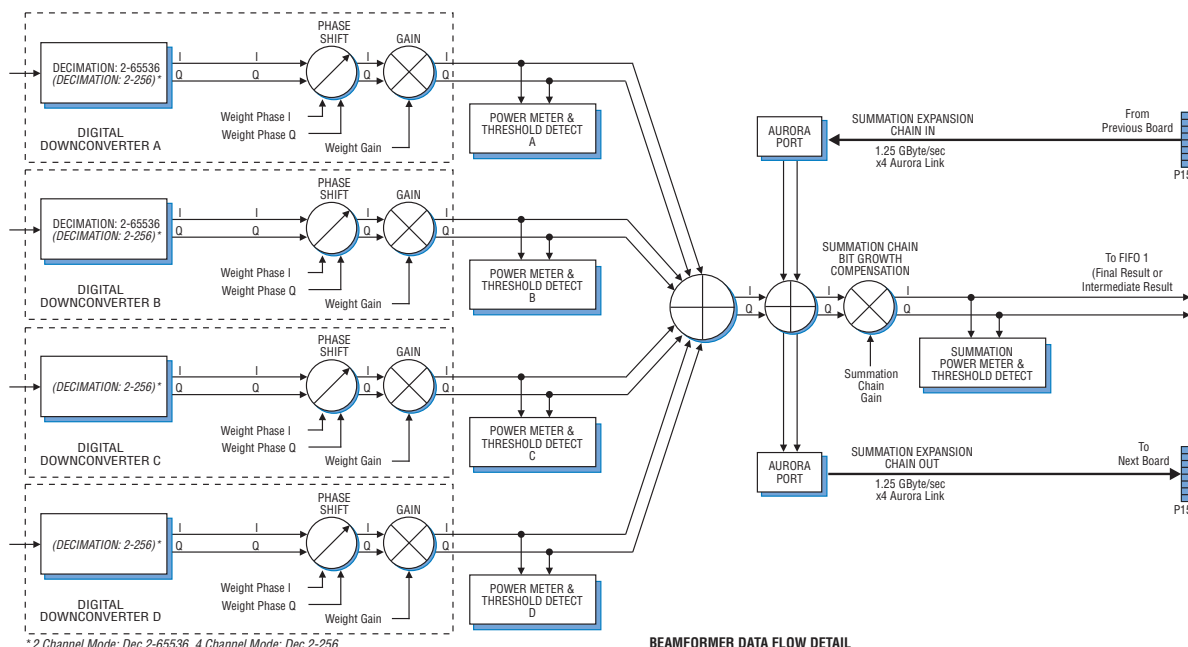
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to two slave 7253Ds or three slave 7353's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI Interface

These models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the boards.

Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported.



BEAMFORMER DATA FLOW DETAIL

Specifications

Model 7253 or 7353: 4-Channel Beamformer

Model 7253D: 8-Channel Beamformer

Model 7253D shown in the Specifications

Front Panel Analog Signal Inputs (8)

Input Type: Transformer-coupled,
front panel female SMC connectors

Transformer Type: Coil Craft
WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8)

Type: Texas Instruments AD5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the

A/Ds can be decimated by any value
between 1 and 4096

Clock Sources (4): Selectable from onboard
crystal oscillator, external reference or
LVPECL clocks

External Clocks (4)

Type: Front panel female SMC connector,
sine wave, 0 to +10 dBm, AC-coupled
50 ohms

Sync/Gate Bus: 26-pin connector, clock/
sync/gate/PPS, input/output LVPECL
bus; one gate/trigger and one sync/PPS
input TTL signal

Digital Downconverter

Type: IP core for Xilinx Virtex-5

Qty of DDC Channels: 4 or 8

Center Frequency Tuning: 8 tuning
words, one for each DDC channel

Center Frequency Tuning Range: DC
to f_s with 32 bit resolution

NCO SFDR: -120 dBFS

Channel Phase Offset Adjustment:
32-bit resolution

Channel Gain Adjustment: 32-bit
resolution

Input Selection for DDC Banks: Any
channel can select any of the four A/Ds

Decimation Range (N):

2-Channel Mode: 2 to 65536

4-Channel Mode: 2 to 256

FIR Filter: Default passband $0.8 \cdot f_s / N$
with 0.2 dB passband ripple and 100 dB
adjacent channel rejection

FIR Filter Coefficients: 18 bits, user-
programmable (default values provided)

Qty FIR Filter Taps: $28 \cdot N / 8$

Output Format: 24 bits I + 24 bits Q

Output Spectrum Modes: Normal or
frequency-reversed

Output Spectrum Offset: No offset or
offset by one-half the output bandwidth

Beamformer

Summation: Four or eight channels on-
board; multiple boards can be summed
via Summation Expansion Chain

Summation Expansion Chain: One
chain in and one chain out link via
XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with
16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion:
32-bit

Output Multiplexer and FIFO

Qty Output FIFOs: Eight

FIFO Source Selection: Independent
multiplexer selects DDC output or A/D

PCI Interface

PCI Bus: 32 or 64 bits at 66 MHz and
32 or 64 bits at 33 MHz

DMA: 8 channel demand-mode and
chaining controller

Local Bus: 64 bits at 33, 66 and 100 MHz

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7253	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - 6U cPCI
7253D	8-Channel DDC with eight 200 MHz, 16-bit A/Ds and Beamformers - 6U cPCI
7353	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - 3U cPCI

Options:

-730	Two-slot heat sink

Contact Pentek for available
options.

New!

Models 7256, 7256D and 7356

Dual/Quad 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - cPCI



Model 7356 Model 7256D



Features

- Complete software radio interface solution
- Two or four 400 MHz, 14-bit A/Ds
- One or two digital upconverters
- Two or four 800 MHz, 16-bit D/As
- Up to 2 GB of DDR2 SDRAM
- Two or four Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Models 7256 and 7356 are cPCI boards that include two 400 MHz A/Ds, 800 MHz D/As and Virtex-5 FPGAs. They consist of one Model 7156 PMC module mounted on a cPCI carrier. The Model 7652 is a 6U cPCI board, while the Model 7356 is a 3U cPCI board. Model 7256D is the same as the Model 7652, except it contains two 7156's rather than one.

A/D Converter Stage

The front end accepts two or four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing, data capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

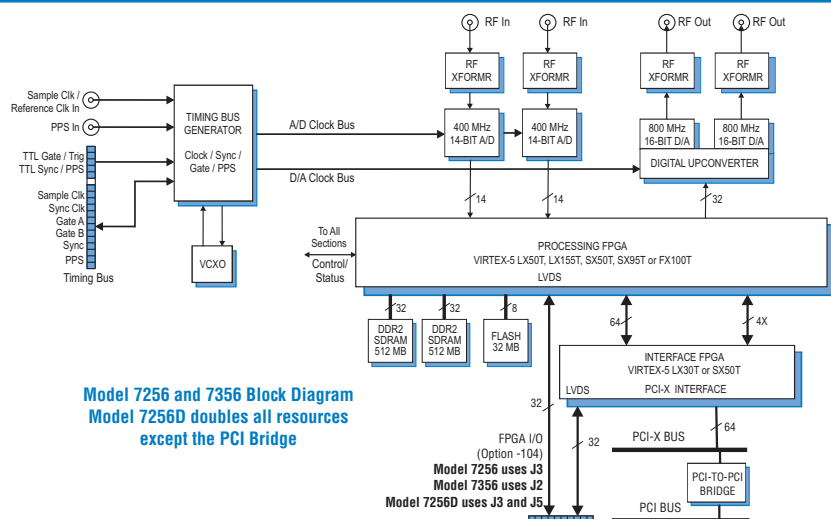
Virtex-5 FPGAs

The architecture includes two or four Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface ➤



Model 7256 and 7356 Block Diagram
Model 7256D doubles all resources
except the PCI Bridge

PCI Interface

All Models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported.

► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 installs the J3 connector (Model 7256) or the J2 connector (Model 7356) with 16 pairs of LVDS connections to the processing FPGA and 16 pairs to the interface FPGA for custom I/O.

With Model 7256D, the option provides an additional 16 pairs of LVDS connections through the J5 connector to the processing FPGA and 16 pairs to the interface FPGA.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to two slave 7256D's and three slave 7356's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Up to four independent 512 MB banks of DDR2 SDRAM are available to the processing FPGAs. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Specifications

Models 7256 or 7356: Dual version

Model 7256D: Quad version

Model 7256D shown in the Specifications

Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4)

Type: TI ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

D/A Converters (4)

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled,

front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 400 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (4)

Processing FPGA: Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Two Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs the J3 and J5 cPCI connectors with 32 pairs of LVDS connections to the processing FPGA and 32 pairs of LVDS connections to the interface FPGA for custom I/O

Environmental Specifications

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7256	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI
7256D	Quad 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI
7356	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI
Options:	
-104	FPGA I/O through cPCI J3 for 7256 or J2 for 7356; cPCI J3 and J5 for 7256D

Contact Pentek for additional available options.

New!

Models 7258, 7258D and 7358

Dual/Quad 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - cPCI



Model 7358 Model 7258D



Features

- Complete software radio interface solution
- Two or four 500 MHz, 12-bit A/Ds
- One or two digital upconverters
- Two or four 800 MHz, 16-bit D/As
- Up to 2 GB of DDR2 SDRAM
- Two or four Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Models 7258 and 7358 are cPCI boards that include two or four 500 MHz A/Ds and 800 MHz D/As and Virtex-5 FPGAs. They consist of one Model 7158 PMC module mounted on a cPCI carrier. The Model 7258 is a 6U cPCI board, while the Model 7358 is a 3U cPCI board. Model 7258D is the same as the Model 7258, except it contains two 7158's rather than one.

A/D Converter Stage

The front end accepts two or four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5463 12-bit 500 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing, data capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

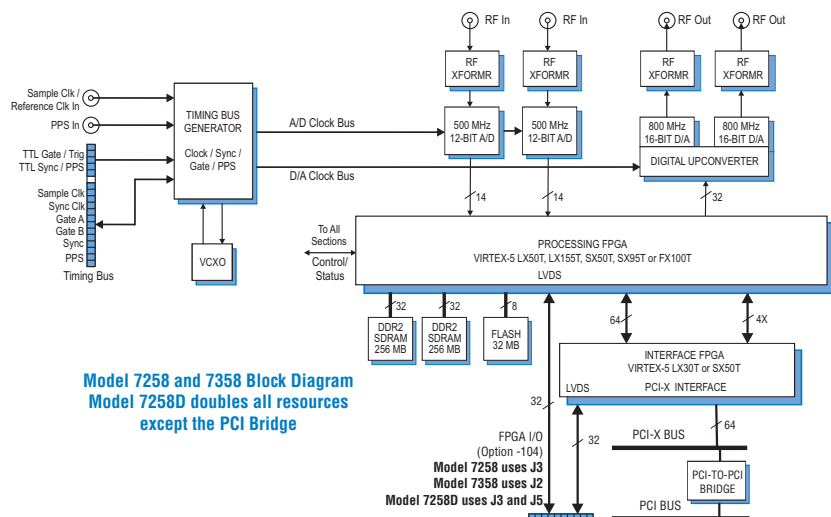
Virtex-5 FPGAs

The architecture includes two or four Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface



Model 7258 and 7358 Block Diagram
Model 7258D doubles all resources except the PCI Bridge

PCI Interface

All Models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported.

Ordering Information

Model	Description
7258	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI
7258D	Quad 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI
7358	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI
Options:	
-104	FPGA I/O through cPCI J3 for 7258 or J2 for 7358; cPCI J3 and J5 for 7258D
-140	1 GB DDR2 SDRAM, Models 7258 and 7358; 2 GB DDR2 SDRAM, Model 7258D

Contact Pentek for additional available options.

► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 installs the J3 connector (Model 7258) or the J2 connector (Model 7358) with 16 pairs of LVDS connections to the processing FPGA and 16 pairs to the interface FPGA for custom I/O.

With Model 7258D, the option provides an additional 16 pairs of LVDS connections through the J5 connector to the processing FPGA and 16 pairs to the interface FPGA.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to two slave 7258D's and three slave 7358's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Two independent 256 MB banks of DDR2 SDRAM are available to the processing FPGA. These can be upgraded to 512 MB banks with option -140.

Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Specifications

Models 7258 or 7358: Dual version

Model 7258D: Quad version

Model 7258D shown in the Specifications
Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4)

Type: TI ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

D/A Converters (4)

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled,

front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 500 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (4)

Processing FPGA: Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Two Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs the J3 and J5 cPCI connectors with 32 pairs of LVDS connections to the processing FPGA and 32 pairs of LVDS connections to the interface FPGA for custom I/O

Environmental Specifications

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

RADAR & SDR I/O - PCI

MODEL	DESCRIPTION
7631A	16-Channel Multiband Receivers with A/Ds and FPGA - PCI
7640	Dual/Multiband Transceivers with FPGA - PCI
7640-420	Dual Wideband DDCs and Interpolation Filter - PCI
7640-430	Transceiver with 256-Channel Narrowband DDC - PCI
7641	Dual Multiband Transceivers with FPGA - PCI
7641-420	Transceiver Dual Wideband DDCs and Interpolation Filter - PCI
7641-430	Transceiver with 256-Channel Narrowband DDC - PCI
7642	Multichannel Transceiver with Virtex-4 FPGAs - PCI
7642-428	Transceiver with four Multiband DDCs and Interpolation Filter - PCI
7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI
7651	256-Channel DDC with four 200 MHz, 16-bit A/Ds - PCI
7652	32-Channel DDC with four 200 MHz, 16-bit A/Ds - PCI
7653	4/2-Channel DDC, four 200 MHz 16-bit A/Ds, Beamformer - PCI
7656	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI
7658	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI
	Customer Information

[RADAR & SDR I/O - PMC/XMC](#)

[RADAR & SDR I/O - CompactPCI](#)

[RADAR & SDR I/O - x16 PCI Express](#)

[RADAR & SDR I/O - x8 PCI Express](#)

[RADAR & SDR I/O - 3U VPX](#)

[Click Here for the PRODUCT SELECTOR](#)

Last updated: November 2010



Features

- Two 80 or 105 MHz, 14-bit A/D converters
- 16 channels of multiband digital downconverters
- 5 kHz to 10 MHz output bandwidth for $f_s = 100$ MHz
- 250 MHz input bandwidth
- Ideal for IF sampling
- User-configurable Xilinx Virtex-II FPGA
- Custom FPGA I/O through a 64-pin DIN connector
- Bypass path allows direct capture of A/D data
- Front panel clock and sync bus
- Synchronization of up to 80 modules (with Model 9190)

General Information

Model 7631A is a general-purpose 16-channel multiband digital receiver half-length PCI board. It includes both a Virtex-II FPGA and two 14-bit A/Ds for signal processing. The 7631A attaches directly to computer boards with PCI bus slots.

Front End

The Model 7631A accepts two analog RF inputs at +4 dBm full scale into 50 ohms on PCI slot panel SMA connectors.

The two inputs are transformer coupled and digitized by AD6645 14-bit A/D converters. The AD6645 operates at a maximum sampling rate of 80 MHz in the standard unit and up to 105 MHz with option -100.

The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, or from an external sample clock supplied through a PCI slot panel SMA connector or the PCI slot panel sync bus.

Digital Downconverters

The 7631A includes four TI/Graychip GC4016 quad multiband digital downconverter chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable channels capable of center frequency tuning from DC to $f_s/2$, where f_s is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from the two A/D converters. A cross-bar switch in each GC4016 allows all 16 channels on the board to select either of the two A/D inputs for flexible switching.

Output Bandwidth

With a 100 MHz sample clock, the useable output bandwidth of each of the downconverter channels is 2.5 MHz. However, since these models deliver parallel digital outputs from the GC4016 into the FPGA, users can take advantage of the GC4016 channel combining mode to join two or four channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.

Since both A/D converters connect directly to the FPGAs, signals with even wider bandwidths can be accommodated.

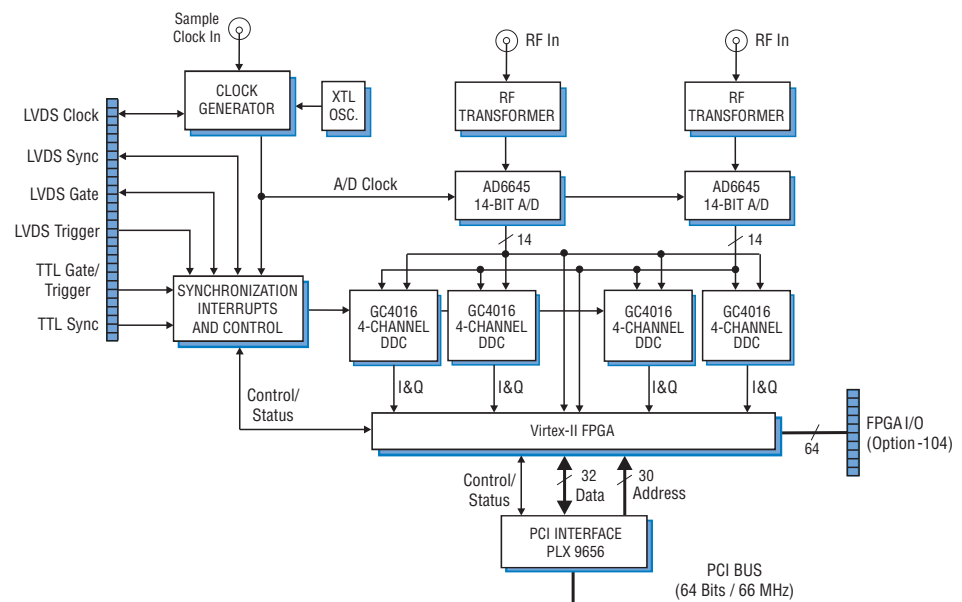
FPGA

The downconverter outputs are delivered to a Xilinx Virtex-II XC2V3000 FPGA which is factory configured to perform various modes of data packing, formatting and channel selection.

Dual port memories in the FPGA provide efficient PCI Bus transfers by buffering downconverter and A/D data.

The A/D outputs are also connected directly to the FPGA so that wideband A/D data can be delivered directly to the baseboard bypassing the downconverters. An A/D decimation mode allows one of every N samples to be written into the FPGA memory, where N is any integer between 1 and 4096. This overcomes the lower frequency limit on the A/D sample clock.

Option -104 installs 64 signal line connections to the XC2V3000 FPGA for custom I/O through a 64-pin DIN connector. ➤



► Synchronization

The front panel clock and sync bus allow one 7631A to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple 7631As.

Up to eight slave 7631A boards can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator. In addition to the LVDS timing bus, the Model 7631A can receive front panel TTL external signals for gate and trigger functions.

Interrupt Sources

The Model 7631A has several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload output codes, transitions on the gate signals, clock loss, buffer swapping, a programmable over-temperature condition or faulty power supply voltage.

The ADM1024 Voltage/Temperature Monitor provides constant monitoring of critical voltages and temperatures and generates an interrupt if values exceed threshold limits which are user-programmable over the PCI interface.

PCI Interface

The FPGA output is connected to a 66 MHz, 64-bit PCI interface capable of 528 MB/sec peak data rates. An industry standard PLX9656 PCI interface chip ensures full conformance to all PCI bus timing specifications.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMA connectors

Transformer Type: Mini-Circuits ADT4-6T

Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 270 MHz

A/D Converters, Standard

Type: Analog Devices AD6645-80

Sampling Rate: 30 MHz to 80 MHz

Internal Clock: 80 MHz crystal osc.

External Clock: 30 to 80 MHz

Resolution: 14 bits

A/D Converters, Option -100

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: 100 MHz crystal osc.

External Clock: 30 to 105 MHz

Resolution: 14 bits

Clock Source: Onboard crystal oscillator, front panel ext clock, or LVDS clock

External Clock

Type: Front panel female SMA connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms impedance

Sync/Gate Bus

Type: 26-pin connector, with one clock, one sync, and two gate input/output LVDS signals; two trigger LVDS inputs; and one sync and one gate input TTL signals

Digital Downconverters

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D outputs are connected to all GC4016's

Output: Parallel complex data

Bypass Mode: Data from the A/D converters can be written directly into the FPGAs at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096

Field Programmable Gate Array

Option -300: Virtex-II XC2V3000

Option -104: Installs 64-pin DIN connector with 64 lines to the XC2V3000 FPGA

Dual Port RAM Data Buffers

Size: 8k x 32 DPRAM

PCI Interface

Type: PLX Technology PCI 9656

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus (FPGA): 32-bit, 66 MHz

Data Transfer Modes: Direct slave mode and DMA mode

PCI Bridge: 64-bit, 66 MHz

Environmental:

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PCI half-length board

Ordering Information

Model	Description
7631A	16-Channel Multiband Receiver with A/Ds and FPGA - PCI

Options:

-100	105 MHz A/D with 100 MHz oscillator
-104	64-pin DIN connector with FPGA I/O
-300	XC2V3000 FPGA



Features

- Complete software radio transceiver solution
- Two 105 MHz 14-bit A/Ds
- Input signal bandwidth up to 40 MHz
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multimodule synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O through a 64-pin DIN connector
- Optional factory-installed IP cores available

General Information

Model 7640 is a half-length PCI multi-band transceiver. It consists of one Model 7140 transceiver mounted on a PCI carrier board. The Model 7640 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on PCI slot panel MMCX connectors at +4 dBm into 50 ohms with transformer coupling into AD6645 14-bit 105 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

A TI/Graychip GC4016 Quad Digital Downconverter accepts either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter (DUC) and dual D/A accepts baseband real or com-

plex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGA

The Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverter, digital upconverter and D/A converters.

Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

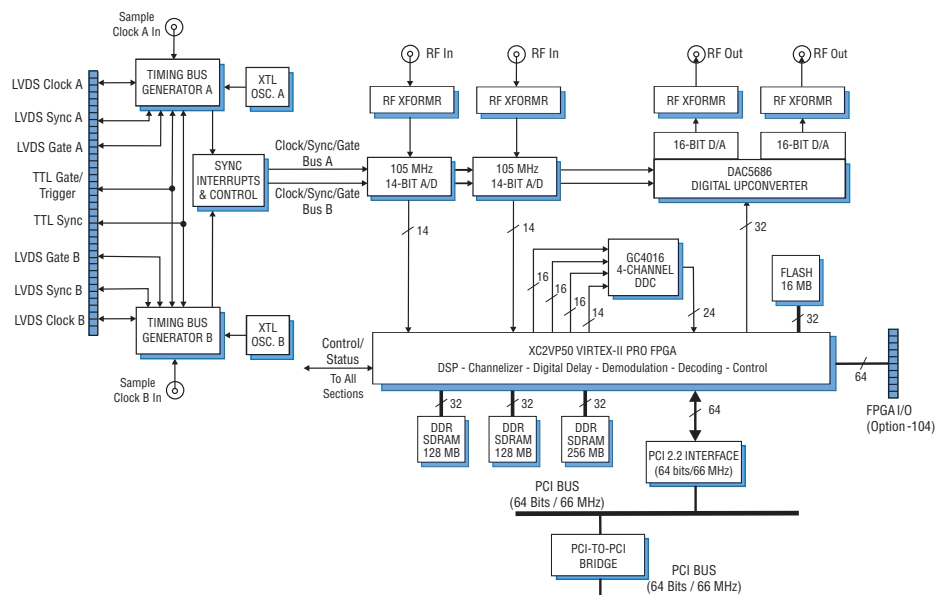
Option -104 adds a 64-pin DIN connector with 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O.

The FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as ➤



► Clocking and Synchronization

the timing source for the A/Ds, the down-converter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7640's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Interface

The Model 7640 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 270 MHz

A/D Converters

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 30 to 105 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

Option -002: -2 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -104: Installs 64-pin DIN connector with 64 lines to the XC2VP50 FPGA

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PCI half-length board

Ordering Information

Model	Description
7640	Dual Multiband Transceiver with FPGA - PCI
Options:	
-002	Full-Scale Output: -2 dBm into 50 ohms; 3 dB Passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillator
-104	FPGA I/O through 64-pin DIN connector
-420	GateFlow Installed core: Dual wideband DDC and interpolation filter
-430	GateFlow Installed core: 256-channel narrowband DDC



General Information

Model 7640-420 is a half-length PCI Transceiver with Dual Wideband DDC and Interpolation Filter. It consists of one Model 7140-420 transceiver mounted on a PCI carrier board. The Model 7640-420 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

The receiver section features two AD6645 105 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other board resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, the board includes Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 downconverter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

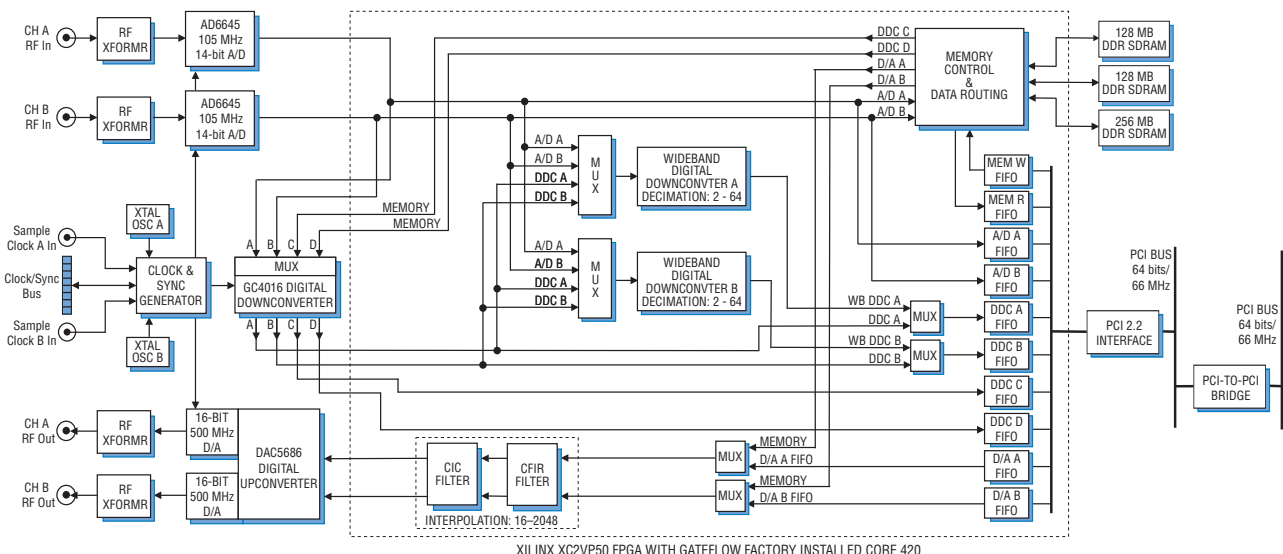
Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of this Model are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤

Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz



XILINX XC2VP50 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 420

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the down-converter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7640-420's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Interface

The Model 7640-420 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Mini-Circuits ADT4-5WT
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 270 MHz

A/D Converters

Type: Analog Devices AD6645-105
Sampling Rate: 30 MHz to 105 MHz
Internal Clock: Crystal oscillator A or B
External Clock: 30 to 105 MHz
Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks
FLASH: One bank of 16 MB.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
Local Bus: 64-bit, 66 MHz
DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard PCI half-length board

Ordering Information

Model	Description
7640-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter - PCI

Contact Pentek for available options



Features

- Complete software radio transceiver solution
- GateFlow Core 430 with 256 channels of narrowband digital downconverters factory-installed
- 256 fully programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

General Information

Model 7640-430 is a half-length PCI transceiver with 256 channels of narrowband DDCs. It consists of one Model 7140-430 transceiver mounted on a PCI carrier board. The Model 7640-430 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

The receiver section features two AD6645 105 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7640-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC

filter coefficient sets are included with the core for all possible decimation settings.

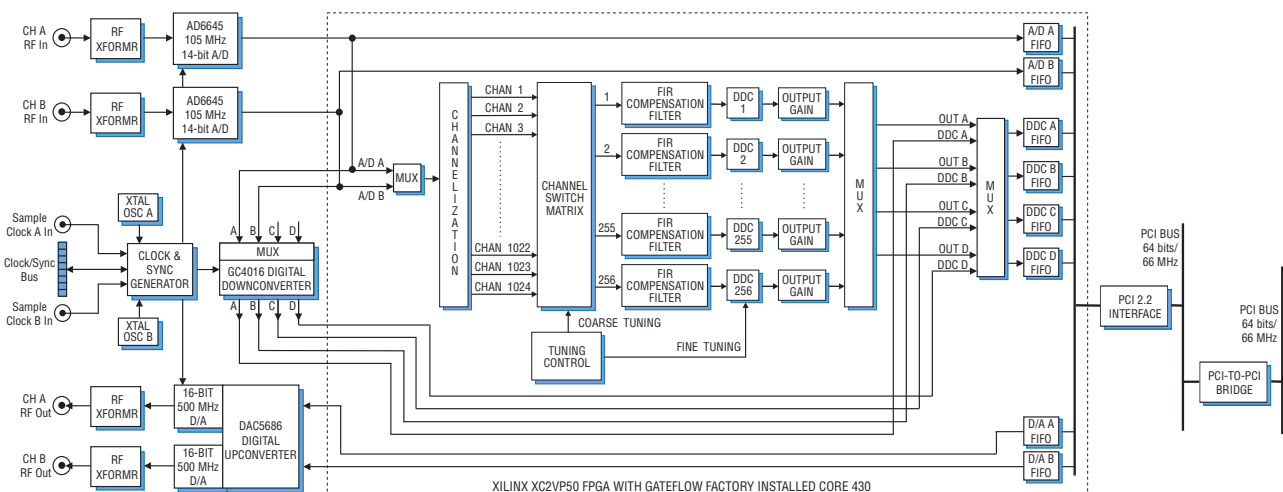
Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2 ³²
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in the Model 7640-430. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 40 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the down-converter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7640-430's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Interface

The Model 7640-430 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Mini-Circuits ADT4-5WT

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 270 MHz

A/D Converters

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 30 to 105 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7640-430	GateFlow Transceiver with 256-Channel Narrowband DDC Core factory-installed - PCI

Contact Pentek for available options



Features

- Complete software radio transceiver solution
- Two 125 MHz 14-bit A/Ds
- Input signal bandwidth up to 50 MHz
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O through a 64-pin DIN connector
- Optional factory-installed IP cores available

General Information

Model 7641 is a half-length PCI multi-band transceiver. It consists of one Model 7141 transceiver mounted on a PCI carrier board. The Model 7641 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on PCI slot panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

A TI/Graychip GC4016 quad digital downconverter accepts either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter (DUC) and dual D/A accepts baseband real or com-

plex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGA

The Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverter, digital upconverter and D/A converters.

Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

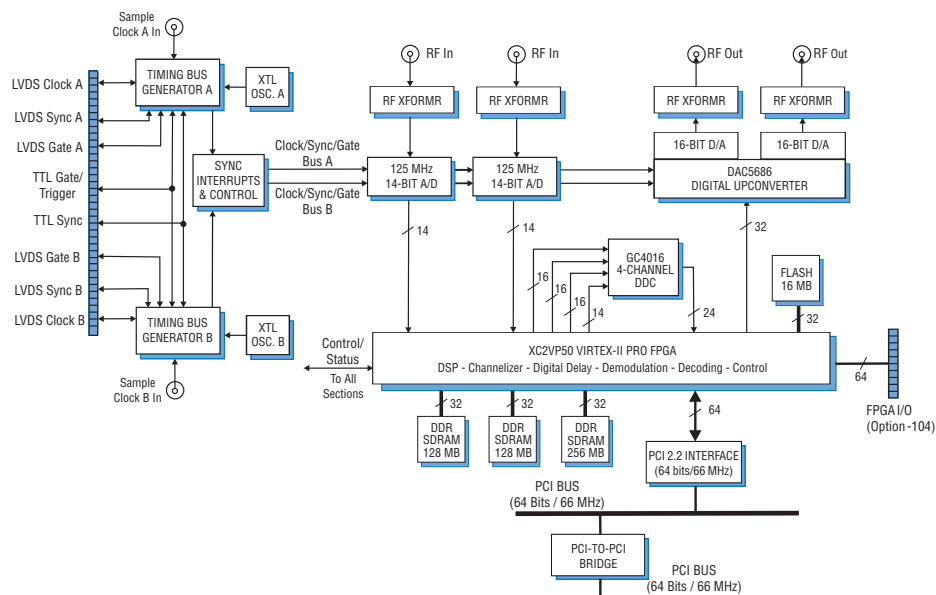
Option -104 adds a 64-pin DIN connector with 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O.

The FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as ➤



► the timing source for the A/Ds, the down-converter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7641's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Interface

The Model 7641 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

Option -002: -2 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -104: Installs 64-pin DIN connector with 64 lines to the XC2VP50 FPGA

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PCI half-length board

Ordering Information

Model	Description
7641	Dual Multiband Transceiver with FPGA - PCI
Options:	
-002	Full-Scale Output: -2 dBm into 50 ohms; 3 dB Passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillator
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through 64-pin DIN connector
-125	125 MHz Bus A and 100 MHz Bus B internal oscillators
-420	GateFlow Installed core: Dual wideband DDC and interpolation filter
-430	GateFlow Installed core: 256-channel narrowband DDC



Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz

General Information

Model 7641-420 is a half-length PCI Transceiver with Dual Wideband DDC and Interpolation Filter. It consists of one Model 7141-420 transceiver mounted on a PCI carrier board. The Model 7641-420 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

The receiver section features two or four LTC2255 125 MHz 14-bit A/D converters and one or two TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, these boards include Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 down-converter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

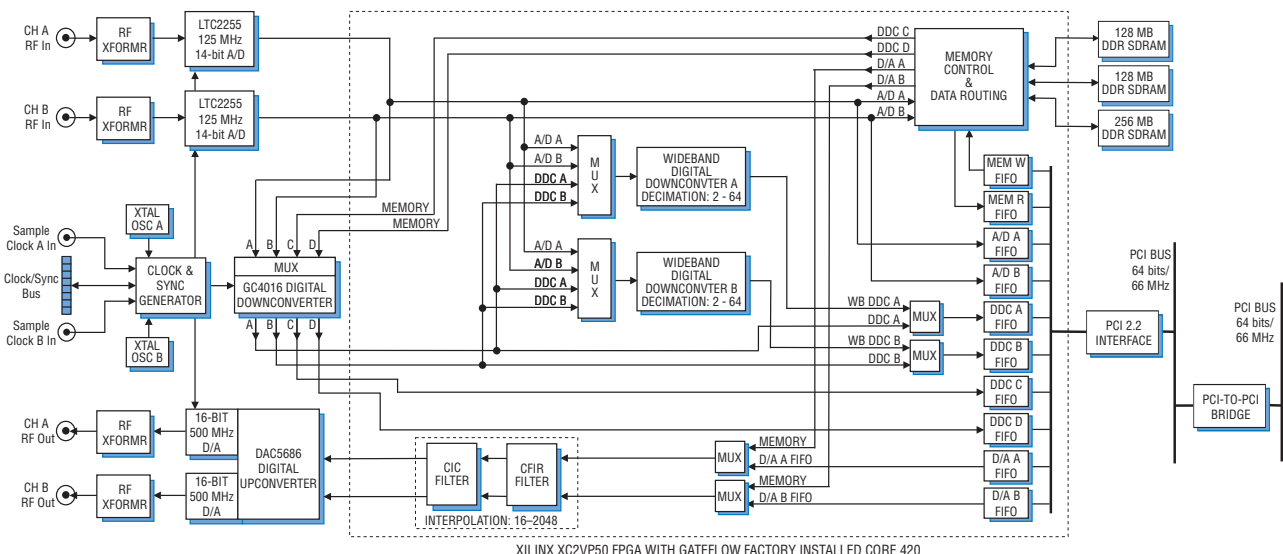
Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of this Model are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the down-converter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7641-420's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

The Model 7641-420 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255
Sampling Rate: 1 MHz to 125 MHz
Internal Clock: Crystal oscillator A or B
External Clock: 1 to 125 MHz
Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks
FLASH: One bank of 16 MB.

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
Local Bus: 64-bit, 66 MHz
DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard PCI half-length board

Ordering Information

Model	Description
7641-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter - PCI

Contact Pentek for available options



ReadyFlow
Board Support Package

GateFlow

Features

- Complete software radio transceiver solution
- GateFlow Core 430 with 256 Channels of Narrowband Digital Downconverters factory-installed
- 256 fully programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

General Information

Model 7641-430 is a half-length PCI transceiver with 256 channels of narrowband DDCs. It consists of one Model 7141-430 transceiver mounted on a PCI carrier board. The Model 7641-430 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory-installed in the 7141-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC

filter coefficient sets are included with the core for all possible decimation settings.

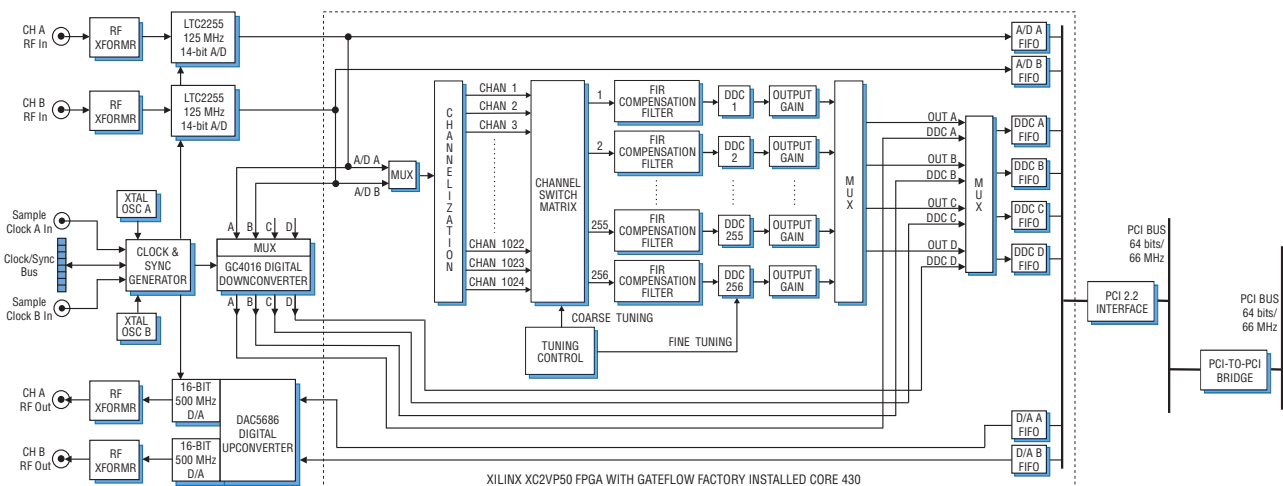
Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2 ³²
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in the Model 7641-430. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the down-converter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7641-430's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Interface

The Model 7641-430 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PCI half-length board

Ordering Information

Model	Description
7641-430	GateFlow Transceiver with 256-Channel Narrowband DDC Core factory installed - PCI

Contact Pentek for available options



Features

- Complete software radio interface solution
- Four 125 MHz 14-bit A/Ds
- One digital upconverter
- One 500 MHz 16-bit D/A
- 768 MB of DDR2 SDRAM
- Xilinx Virtex-4 FPGAs
- Up to 2.0 seconds of delay or data capture at 125 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-4 FPGA for custom I/O
- Optional factory-installed IP Cores available

General Information

Model 7640 is a half-length PCI multichannel transceiver. It consists of one Model 7142 transceiver mounted on a PCI carrier board. The Model 7642 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

The Model 7642 architecture includes two Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can include their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

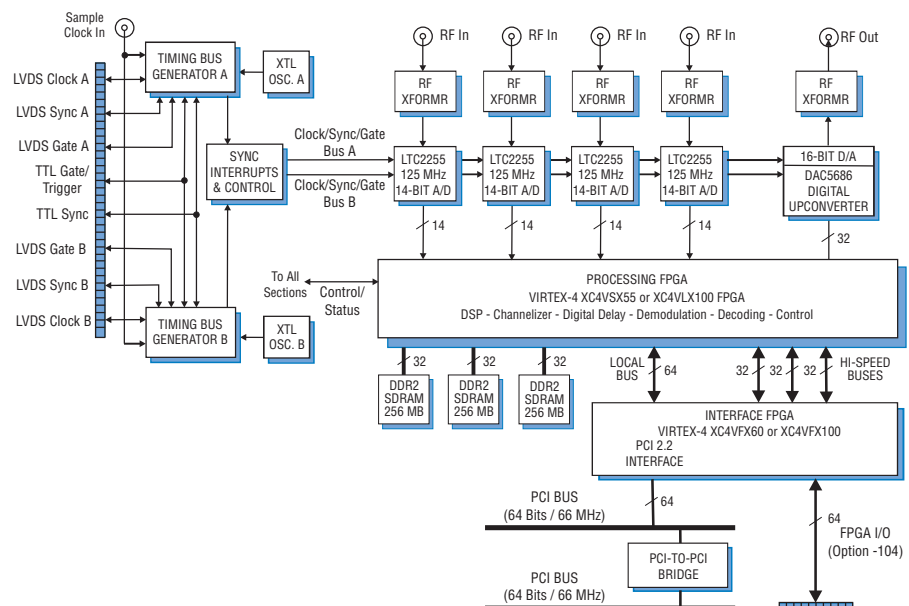
The Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission.

For applications requiring more FPGA logic cells, the Model 7642 can be optionally configured with an XC4VLX100 in place of the XC2VSX55 for 110,592 logic cells.

A second Virtex-4 FPGA provides board interfaces including PCI and serial I/O. The XC4VFX60 FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. The Model 7642 can be optionally configured with a XC4VFX100 in place of the XC4VFX60.

Option -104 installs a 64-pin DIN connector with 32 pairs of LVDS lines to the XC4VFX60/100 FPGA for custom I/O. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds and the upconverter and the D/A. Two internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 7642s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

The Model 7642 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal osc.

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms (other options available)

3 dB Passband: 60 kHz to 300 MHz (other options available)

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: One Xilinx Virtex-4 XC4VSX55 & one Xilinx Virtex-4 XC4VFX60

Option -100: XC4VFX100 replaces XC4VFX60

Option -110: XC4VLX100 replaces XC4VSX55

Custom I/O

Option -104: Installs 64-pin DIN connector with 64 lines to the XC4VFX60/100 FPGA

Memory

DDR2 SDRAM: 768 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board

Ordering Information

Model Description

7642 Multichannel Transceiver with Virtex-4 FPGAs - PCI

Options:

-100	XC4VFX100 replaces XC4VFX60
-104	FPGA I/O through 64-pin DIN connector
-110	XC4VLX100 replaces XC4VSX55
-428	Four multiband DDCs and interpolation filter, factory-installed core



Features

- Complete software radio transceiver solution
- GateFlow IP Core 428, with four high-performance multiband DDCs and Interpolation Filter, factory-installed
- Improved dynamic range
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4

General Information

Model 7642-428 is a half-length PCI Transceiver with four multiband DDCs and Interpolation Filter. It consists of one Model 7142-428 transceiver mounted on a PCI carrier board. The Model 7642-428 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other module resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating

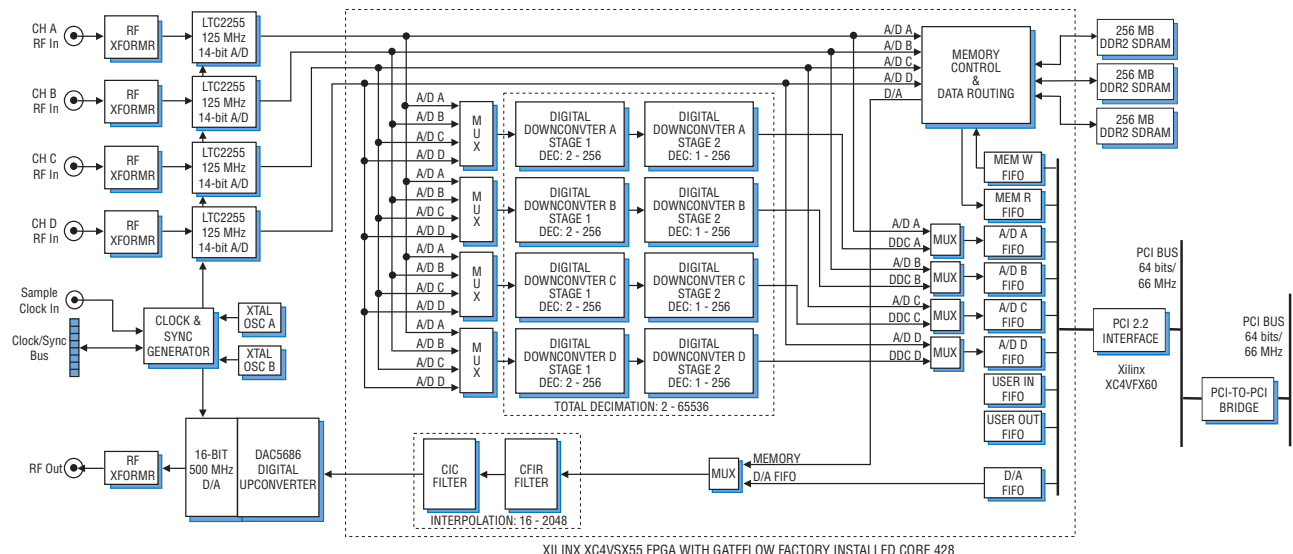
FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds and the upconverter and the D/A. Two internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7642-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

PCI Interface

The Model 7642-428 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal osc.

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: One Xilinx Virtex-4 XC4VSX55 and one Xilinx Virtex-4 XC4VFX60

Memory

DDR2 SDRAM: 768 MB in three banks

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Local Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI card

Ordering Information

Model	Description
7642-428	Gateflow Transceiver with four DDCs and Interpolation Filter factory-installed - PCI

Contact Pentek for available options

New!

Model 7650

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI



General Information

Model 7650 is a half-length PCI Quad 200 MHz A/D. It consists of one Model 7150 Quad A/D mounted on a PCI carrier board. The Model 7650 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA,

programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7650 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but additional processing resources up to an additional 640 DSP48E Slices.

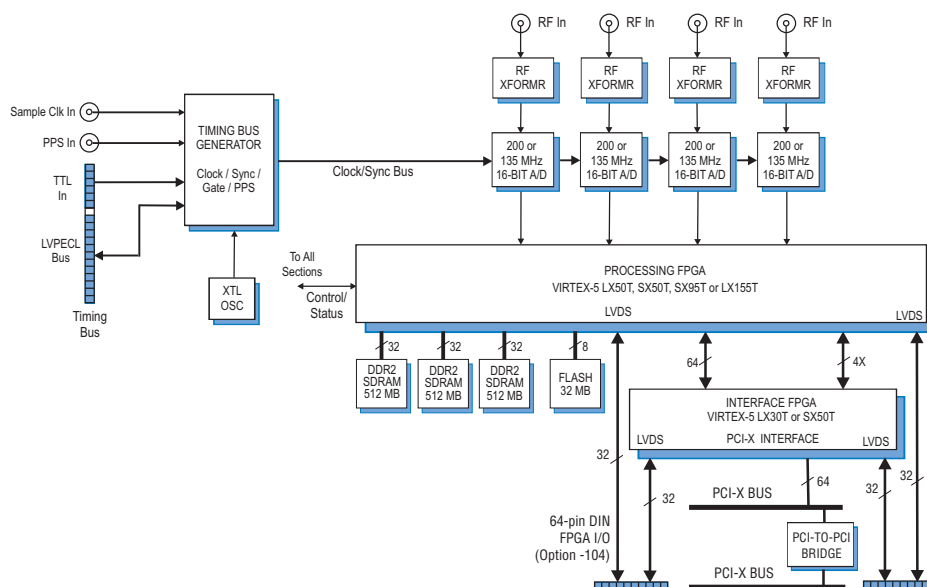
Option -104 installs a 64-pin DIN connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ➤

Features

- Complete software radio interface solution
- Four or 200 MHz, 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O



► Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI-X Interface

The Model 7650 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, the Model 7650 can be optionally factory-configured with x4 PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs a 64-pin DIN connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs to the interface FPGA for custom I/O

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI card

Ordering Information

Model	Description
7650	Quad 200 MHz, 16-bit A/D with two Virtex-5 FPGAs - PCI

Options:

-104	FPGA I/O through a 64-pin DIN connector

Contact Pentek for additional available options.

New!

Model 7651

256-Channel DDC with four 200 MHz, 16-bit A/Ds - PCI



Features

- 256 channels of DDC
- Four 200 MHz 16-bit A/Ds
- Independent tuning for each channel
- DDC decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization

General Information

Model 7651 is a high-speed software radio half-length PCI board. It consists of one Model 7151 Quad A/D digitizer with a factory-installed high-performance 256-channel DDC IP Core mounted on a PCI carrier board. The Model 7651 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7651 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 256 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

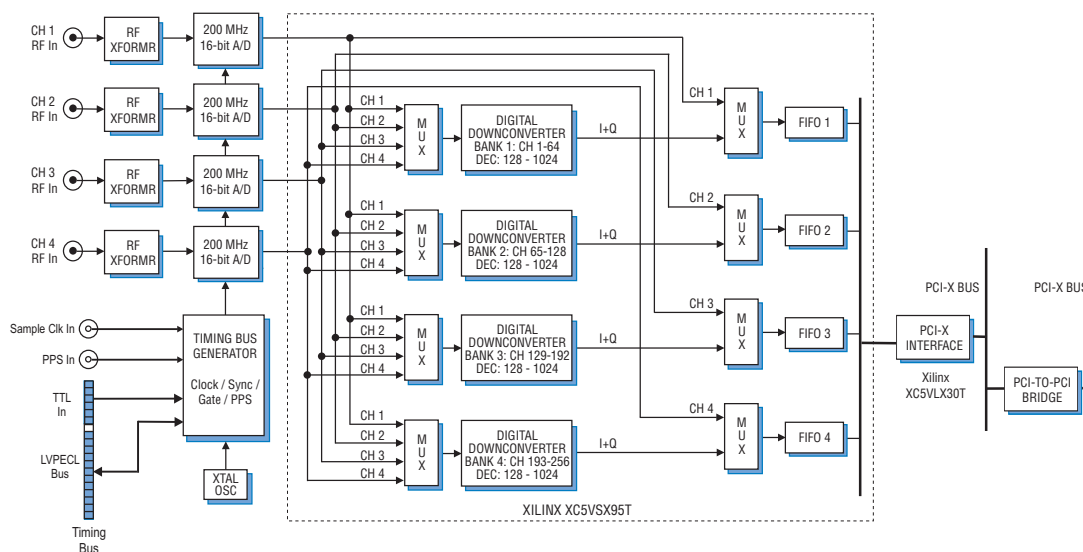
The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wide-band A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI-X bus. ➤



New!

► Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7651s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7651 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the board.

Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Local Bus: 64-bit, 66 MHz

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI card

Ordering Information

Model	Description
7651	256-Channel DDC with four 200 MHz, 16-bit A/Ds - PCI

Options:

-732	Two-slot heat sink

Contact Pentek for available options.



Features

- 32 channels of DDC in four banks of 8 channels
- Four 200 MHz, 16-bit A/Ds
- Independent 32-bit DDC tuning for all 32 channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths from 20 kHz to 10 MHz
- Common decimation factor within each DDC bank
- Different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multiboard synchronization

General Information

Model 7652 is a high-speed software radio half-length PCI board. It consists of one Model 7152 Quad A/D digitizer with a factory-installed high-performance 32-channel DDC IP Core mounted on a PCI carrier board. The Model 7652 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7652 employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 32 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

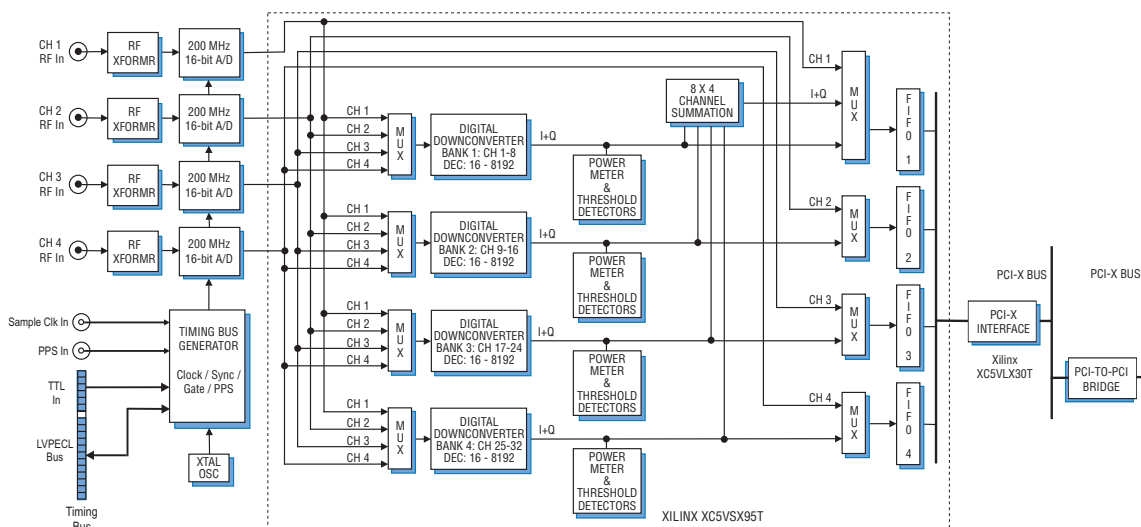
All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

The 7652 features 32 power meters that continuously measure the individual average power output of each of the 32 DDC channels. The time constant of the averaging interval for each meter is programmable up to 16K samples. In addition, 32 threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤



► Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI-X bus.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three 7652s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7652 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the board.

Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, and XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface in the standard unit; optional FPGA: XC5VSX50T

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Local Bus: 64-bit, 66 MHz

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board

Ordering Information

Model	Description
7652	32-Channel DDC with four 200 MHz, 16-bit A/Ds - PCI

Options:

-732	Two-slot heat sink

Contact Pentek for available options.

New!

Model 7653

4/2-Ch. DDC, four 200 MHz 16-bit A/Ds, Beamformer - PCI



ReadyFlow
Board Support Package

Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- Four 200 MHz, 16-bit A/Ds
- 2 or 4 Channels of DDC
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7653 is a 4-channel, high-speed software radio board designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

The Model 7653 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7653 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency.

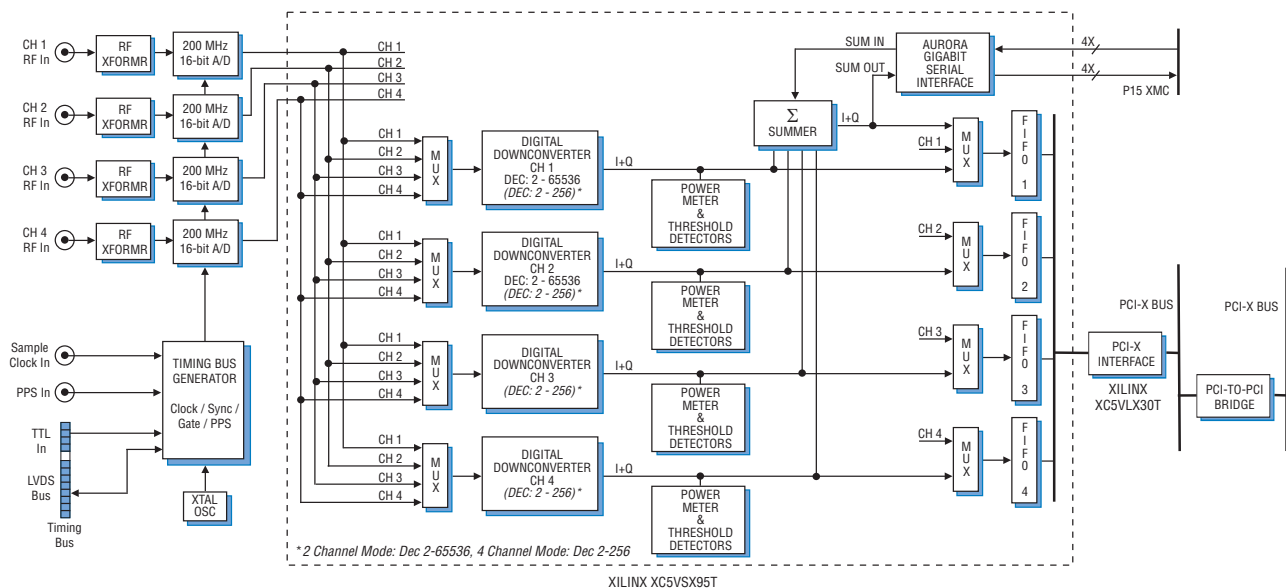
Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N .

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications. ➤



XMC Interface

For large systems, multiple 7653's can be chained together via a built-in Xilinx Aurora interface through the P15 XMC connector.

This link creates a board-to-board summation expansion chain for creating larger multi-channel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

► Beamformer

In addition to the A/Ds and DDCs, the 7653 includes essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable-gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCI-X bus.

For larger systems, multiple 7653's can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates an x4 sum output stream to the next board through the P15 XMC connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI-X bus.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

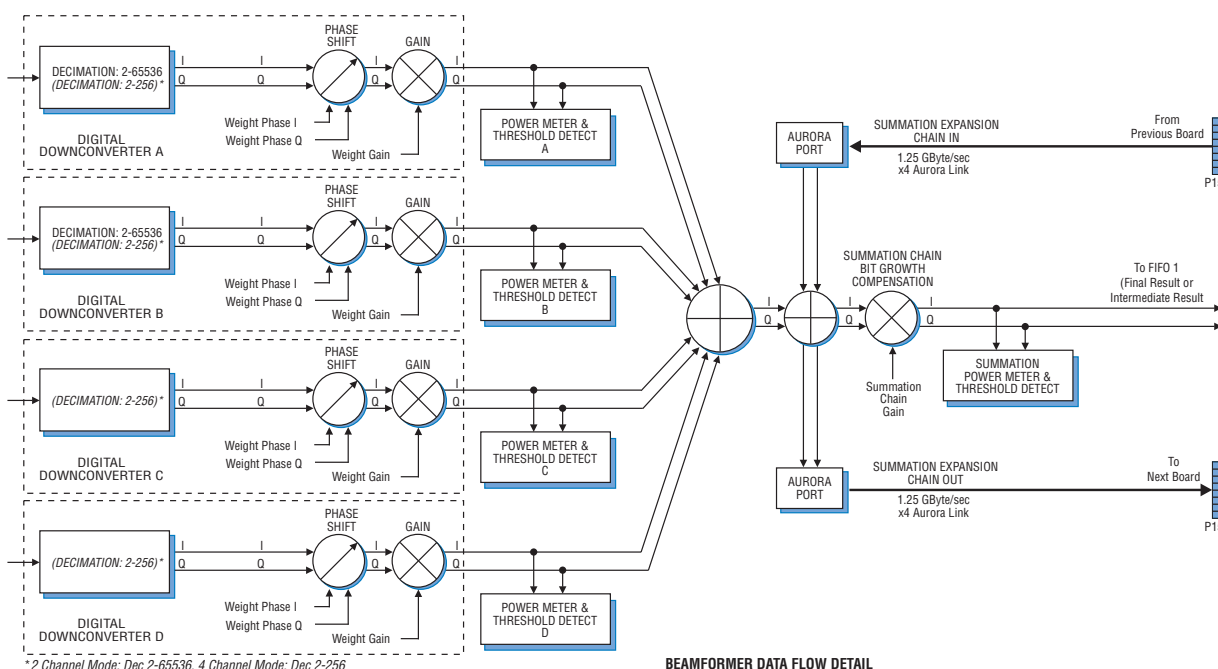
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three 7653's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7653 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the board.

Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.



Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillator, external reference or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS, input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Digital Downconverter

Type: IP core for Xilinx Virtex-5

Qty of DDC Channels: 2 or 4

Center Frequency Tuning: 4 tuning words, one for each DDC channel

Center Frequency Tuning Range: DC to f_s with 32 bit resolution

NCO SFDR: -120 dBFS

Channel Phase Offset Adjustment: 32-bit resolution

Channel Gain Adjustment: 32-bit resolution

Input Selection for DDC Banks: Any channel can select any of the four A/Ds

Decimation Range (N):

2-Channel Mode: 2 to 65536

4-Channel Mode: 2 to 256

FIR Filter: Default passband $0.8 \cdot f_s / N$ with 0.2 dB passband ripple and 100 dB adjacent channel rejection

FIR Filter Coefficients: 18 bits, user-programmable (default values provided)

Qty FIR Filter Taps: $28 \cdot N / 8$

Output Format: 24 bits I + 24 bits Q

Output Spectrum Modes: Normal or frequency reversed

Output Spectrum Offset: No offset or offset by one-half the output bandwidth

Beamformer

Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain

Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion: 32-bit

Output Multiplexer and FIFO

Qty Output FIFOs: Four

FIFO Source Selection: Independent multiplexer selects DDC output or A/D

PCI Interface

PCI-X Bus: 64 bits, 100 MHz and 64 or 32 bits at 33 or 66 MHz

DMA: 4-channel demand-mode and chaining controller

Local Bus: 64-bit, 66 MHz

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board

Ordering Information

Model	Description
7653	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - PCI

Options:

-732	Two-slot heat sink

Contact Pentek for available options.

New!

Model 7656

Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI



Features

- Complete software radio interface solution
- Two 400 MHz, 14-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7656 is a half-length PCI board that includes two 400 MHz A/Ds, 800 MHz D/As and Virtex-5 FPGAs. It consists of one Model 7156 PMC module mounted on a PCI carrier board. The Model 7656 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing, data capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

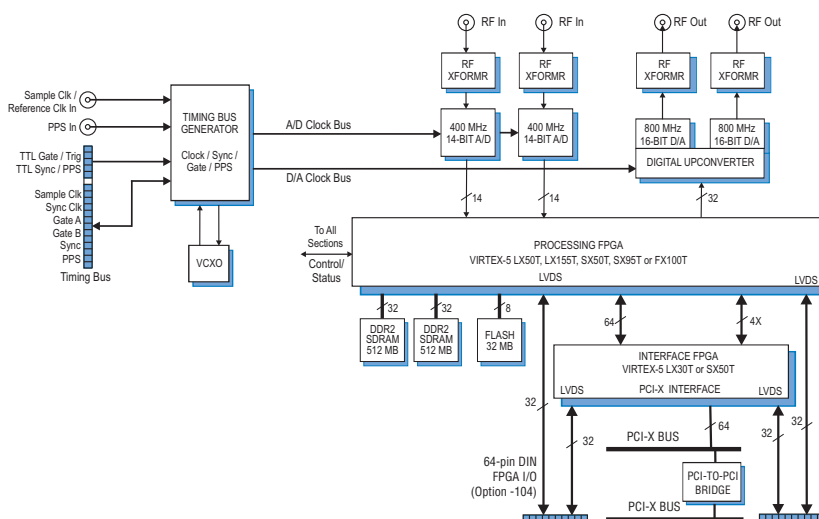
Virtex-5 FPGAs

The Model 7656 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface ➤



► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 adds a 64-pin DIN connector with 16 pairs of LVDS connections to each FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 7656's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

PCI-X Interface

The Model 7656 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled,

front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 400 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs a 64-pin DIN connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA mapped as two 16-bit read/write registers

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board

Ordering Information

Model	Description
7656	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI

Options:

-104	FPGA I/O through a 64-pin DIN connector

Contact Pentek for additional available options.

New!

Model 7658

Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI



Features

- Complete software radio interface solution
- Two 500 MHz, 12-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7658 is a half-length PCI board that includes two 500 MHz A/Ds, 800 MHz D/As and Virtex-5 FPGAs. It consists of one Model 7158 PMC module mounted on a PCI carrier board. The Model 7658 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5463 12-bit 500 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing, data capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

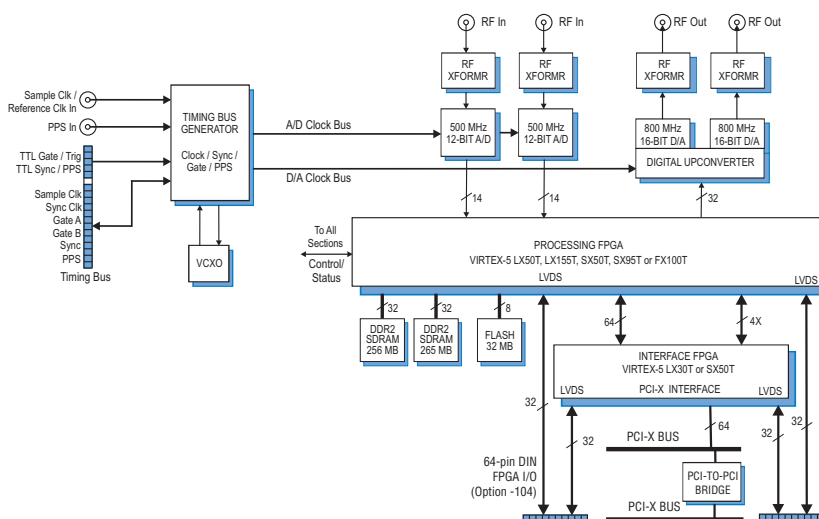
Virtex-5 FPGAs

The Model 7658 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface



► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 adds a 64-pin DIN connector with 16 pairs of LVDS connections to each FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 7658's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Two independent 256 MB banks of DDR2 SDRAM are available to the processing FPGA. These can be upgraded to 512 MB banks with option -140. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

PCI-X Interface

The Model 7658 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 500 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs a 64-pin DIN connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA mapped as two 16-bit read/write registers

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board

Ordering Information

Model	Description
7658	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI

Options:

-104	FPGA I/O through a 64-pin DIN connector
-140	1 GB DDR2 SDRAM

Contact Pentek for additional available options.

RADAR & SDR I/O - x16 PCI Express

MODEL	DESCRIPTION
7741	Dual/Quad Multiband Transceivers with FPGA - Full-length PCIe
7741-420	Transceivers w. Dual/Quad Wideband DDCs and Interpolation Filter - Full-length PCIe
7741-430	Transceivers with 256/512-Channel Narrowband DDC - Full-length PCIe
7742	Multichannel Transceivers with Virtex-4 FPGAs - Full-length PCIe
7742-428	Transceivers with 4/8 Multiband DDCs and Interpolation Filters - Full-length PCIe
7750	Quad or Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length PCIe
7751	256- or 512-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - Full-length PCIe
7752	32- or 64-Channel DDC with 4 or 8 200 MHz, 16-bit A/Ds - Full-length PCIe
7753	4/8-Channel DDC, 4/8 200 MHz 16-bit A/Ds, Beamformer - Full-length PCIe
7756	Dual/Quad 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe
7758	Dual/Quad 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe
	Customer Information

[RADAR & SDR I/O - PMC/XMC](#)

[RADAR & SDR I/O - CompactPCI](#)

[RADAR & SDR I/O - PCI](#)

[RADAR & SDR I/O - x8 PCI Express](#)

[RADAR & SDR I/O - 3U VPX](#)

[Click Here for the PRODUCT SELECTOR](#)

Last updated: November 2010



Model 7741D

Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Two or four 125 MHz 14-bit A/Ds, and two or four 500 MHz 16-bit D/As
- Up to eight digital downconverters and two digital upconverters
- Up to 1 GB of DDR SDRAM
- Up to 2.56 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization

General Information

Model 7741 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It is available with either two A/D and two D/A converters (Model 7741) or four A/D and four D/A converters (Model 7741D), and is capable of bandwidths to 50 MHz and above. It attaches directly to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts two or four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling for the LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

The 7741 features one or two TI/Graychip GC4016 quad digital downconverters, each accepting either four 14-bit or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/Ds, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each

channel ranges from 5 kHz up to 2.5 MHz. By combining channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter and dual D/A is attached to each FPGA, accepting baseband real or complex data streams with signal bandwidths up to 40 MHz.

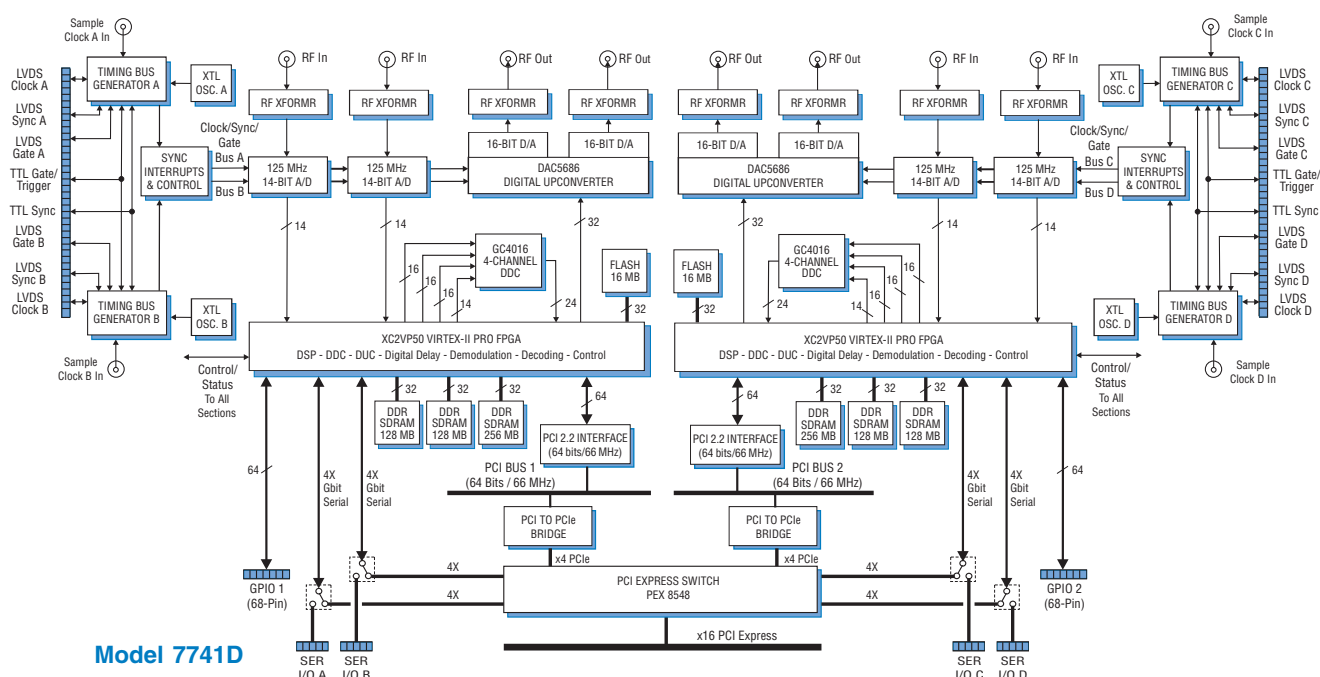
When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two-channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGAs

One or two Xilinx XC2VP50 Virtex-II Pro FPGAs serve as control and status engines with data and programming interfaces to each of the on-board resources including the A/D converters, digital downconverter, digital upconverter and D/A converters.

Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. Option -104 adds up to 64 pairs of LVDS connections to each Virtex-II Pro FPGA for custom I/O. Option -5xx adds up to four full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols. ▶



► Clocking and Synchronization

Two independent internal timing buses per FPGA can provide either a single clock or two different clock rates for the corresponding input and output signals.

Each timing bus includes a clock, sync, and gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the associated A/Ds, down-converter, upconverter and D/As. Two external reference clocks or two internal clocks may be used for each timing bus.

One or two front panel 26-pin LVDS Clock/Sync connectors allow multiple modules to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7741's can be driven from each LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available to each FPGA (to 1 GB max.). Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within each FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Express Interface

The 7741 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to each FPGA, as well as one x4 connection to each 64-bit PCI interface.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal osc. (2 per A/D)

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

Option -002: -2 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clocks

Type: Female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohm

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -104: 64 lines per FPGA

Memory

DDR SDRAM: 512 MB in three banks per FPGA (maximum 1 GB)

FLASH: One bank of 16 MB per FPGA (maximum 32 MB)

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: two x4 ports per FPGA

one x4 port per PCI bus

one x16 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

Model	Description
7741	Dual Multiband Transceiver with FPGA - Full-length x16 PCIe
7741D	Quad Multiband Transceiver with FPGA - Full-length x16 PCIe
Options:	
-002	Full-scale output: -2 dBm into 50 ohms; 3 dB passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA (one for Model 7741, two for 7741D)
-100	All oscillators 100 MHz
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through GPIO connector(s)
-125	125 MHz Bus A/C and 100 MHz Bus B/D internal oscillators
-420	Dual wideband DDC and digital interpolation filter cores, factory-installed in one FPGA (Model 7741) or two FPGAs (7741D)
-430	256-channel narrowband DDC core, factory-installed in one FPGA (Model 7741) or two FPGAs (7741D)
-5xx	Gigabit Serial I/O - two full duplex 4X paths (Model 7741) or four full duplex 4X paths (7741D)



Model 7741D-420



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz

General Information

Model 7741-420 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It is available with either two A/D and two D/A converters (Model 7741-420) or four A/D and four D/A converters (Model 7741D-420). These Models attach directly to motherboards with full-length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

The receiver section features two or four LTC2255 125 MHz 14-bit A/D converters and one or two TIGC4016 quad multiband digital downconverters. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, these boards include Pentek's GateFlow installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 downconverter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and

formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

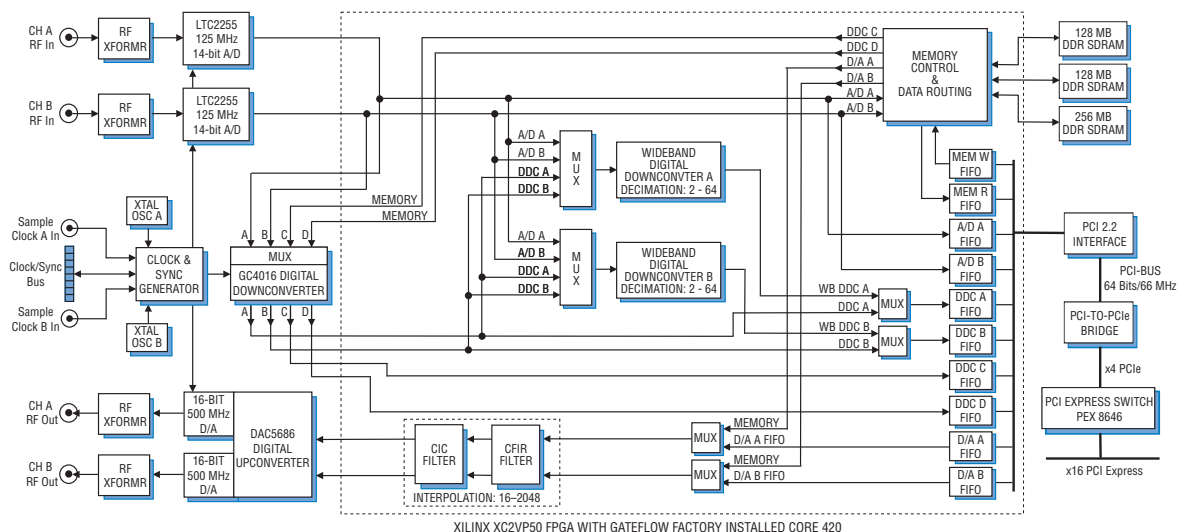
A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of these Models are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤

Block Diagram, Model 7741-420. Model 7741D-420 doubles all resources except the PCIe switch.



XILINX XC2VP50 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 420

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7741D-420's or seven 7741-420's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7741-420 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to each FPGA, as well as one x4 connection to each 64-bit PCI interface.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: Up to 1 GB in six banks

FLASH: Up to 32 MB in two banks.

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port per PCI bus; one x16 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

Model	Description
7741-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - Full-length x16 PCIe
7741D-420	GateFlow Transceiver with four Wideband DDCs and two Interpolation Filters factory-installed - Full-length x16 PCIe

Contact Pentek for available options



Model 7741D-430



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- GateFlow Core 430 with 256 or 512 Channels of Narrowband Digital Downconverters factory-installed
- 256 or 512 programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

General Information

Model 7741-430 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It is available with either two A/D and two D/A converters (Model 7741-430) or four A/D and four D/A converters (Model 7741D-430). These Models attach directly to motherboards with full-length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7141-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter

coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

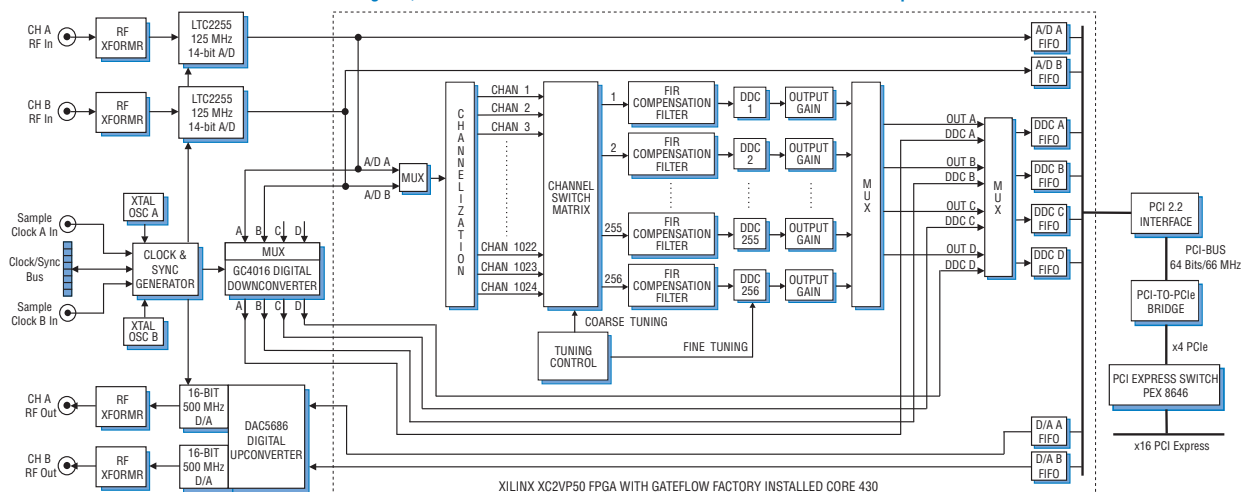
Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2 ³²
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in these Models. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any interger value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤

Block Diagram, Model 7741-430. Model 7741D-430 doubles all resources except the PCIe switch.



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7741-430's, or four slave 7741D-430's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

PCI Express Interface

The 7741-430 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to each FPGA, as well as one x4 connection to each 64-bit PCI interface.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: Up to 1 GB in six banks

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port per PCI bus; one x16 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

Model	Description
7241-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - Full-length x16 PCIe
7241D-430	GateFlow Transceiver with 512-Channel Narrowband DDC factory-installed - Full-length x16 PCIe

Contact Pentek for available options



Model 7742D



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Switched fabric support
- 125 MHz 14-bit A/Ds
- Digital upconverters
- 500 MHz 16-bit D/As
- Up to 1.5 GB of DDR2 SDRAM
- Xilinx Virtex-4 FPGAs
- LVDS clock/sync bus for multimodule synchronization
- Optional factory-installed IP Cores available

General Information

Model 7742 is a multichannel data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds with one upconverter and D/A converter (Model 7742), or eight A/Ds with two upconverters and D/As (Model 7742D). It attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computers.

A/D Converter Stage

The front end accepts four or eight full scale analog HF or IF transformer-coupled inputs on front panel MMCX connectors at +10 dBm into 50 ohms into Linear Technology LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into a Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

The 7742 features one or two TI DAC5686 digital upconverters (DUCs) and D/As. Each accepts a baseband real or complex data stream from its attached FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, the DAC5686 interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs up to 320 MHz to the 16-bit D/A converter. If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

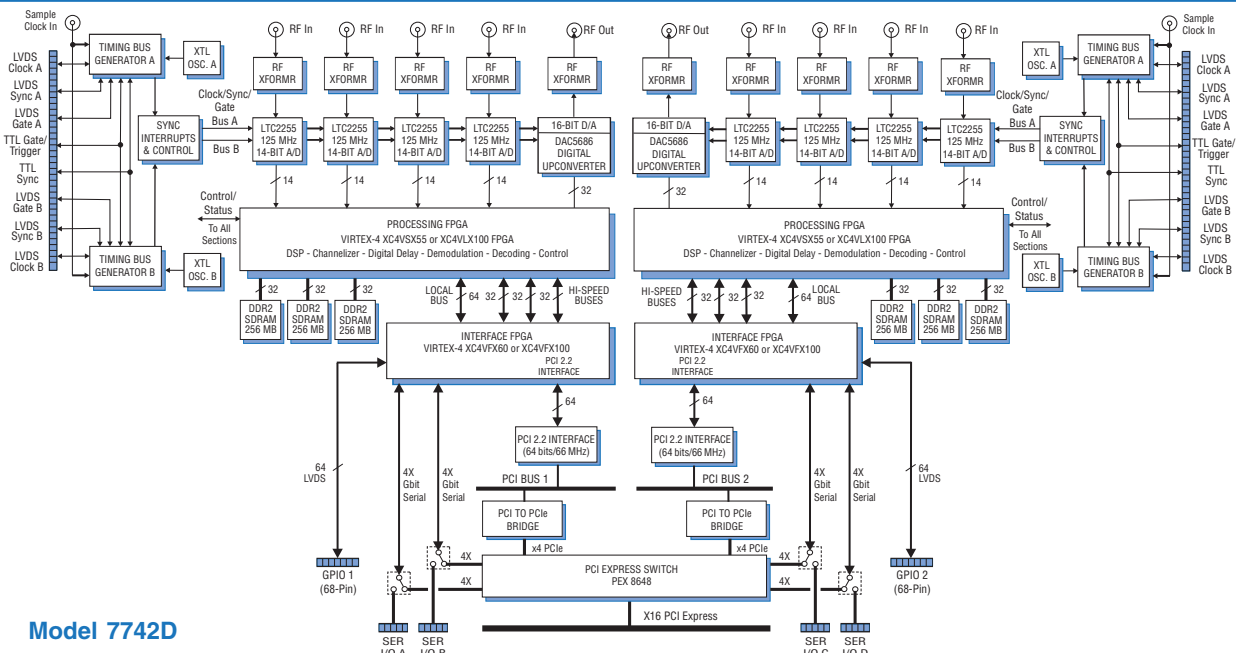
The 7742 architecture includes two (Model 7742) or four (Model 7742D) Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can include their own custom IP, and integrate it with factory-shipped functions using a Pentek GateFlow FPGA Design Kit.

Each Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for implementing functions such as demodulation/modulation, digital delay and channelization. For applications requiring more FPGA logic cells, these Models can be optionally configured with XC4VLX100 in place of each XC2VVSX55 for up to 221,184 logic cells.

One or two Virtex-4 XC4VFX60 Interface FPGAs provide board interfaces including PCI and serial I/O. Each Interface FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. These Models can be optionally configured with XC4VFX100 in place of each FX60.

Option -104 installs a GPIO connector with 32 pairs of LVDS connections to each XC4VFX60/100 Interface FPGA for custom I/O. ➤



Model 7742D

PCI Express Interface

The 7742 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two optional x4 PCIe connections to each SX55/LX100 FPGA, and one x4 connection to each 64-bit PCI interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Ordering Information

Model Description

7742	Multichannel Transceiver with four A/Ds, one D/A and Virtex-4 FPGAs - Full-length x16 PCIe
7742D	Multichannel Transceiver with eight A/Ds, two D/As and Virtex-4 FPGAs - Full-length x16 PCIe

Options:

-100	XC4VFX100 replaces XC4VFX60
-104	FPGA I/O through GPIO connector(s)
-110	XC4VLX100 replaces XC4VSX55
-428	Four multiband DDCs and interpolation filter, factory-installed core in each processing FPGA
-5xx	Gigabit Serial I/O - two full duplex 4X paths (Model 7742) or four full duplex 4X paths (7742D)

Clocking and Synchronization

Two independent internal timing buses per bank of four A/Ds can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the associated A/Ds, upconverter and D/A. Internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

One or two front panel 26-pin LVDS Clock/Sync connectors allow multiple modules to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, each LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7742s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to each SX55 or LX100 FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255
Sampling Rate: 1 MHz to 125 MHz
Internal Clock: 125 MHz crystal osc.
External Clock: 1 to 125 MHz
Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock divided by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connector
Full Scale Output: +4 dBm into 50 ohms (other options available)
3 dB Passband: 60 kHz to 300 MHz (other options available)

Digital Upconverter

Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-4 XC4VSX55 & Xilinx Virtex-4 XC4VFX60
Option -100: XC4VFX100 replaces XC4VFX60
Option -110: XC4VLX100 replaces XC4VSX55

Custom I/O

Option -104: Adds GPIO connector with 32 lines to each XC4VFX60/100 FPGA

Memory

DDR2 SDRAM: 768 MB in three banks per SX55/LX100 FPGA (1.5 GB max.)

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz
DMA: 9 channel demand-mode and chaining controller per PCI bus
PCIe Interface: Gen. 2, x16 width
Ports: one x4 port per PCI bus
 one x16 port to PCIe motherboard;
 two optional 4X ports per Interface
 FPGA for other gigabit protocols

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Full-length PCIe, 4.38 in. x 12.3 in.



Model 7742D-428



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- GateFlow IP Core 428, with four or eight high-performance multiband DDCs and one or two Interpolation Filters, factory-installed
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4

General Information

Model 7742-428 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It is available with either four A/D and one D/A converters (Model 7742-428) or eight A/D and two D/A converters (Model 7742D-428). These Models attach directly to motherboards with full-length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other module resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The

DDCs consist of two cascaded decimating FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

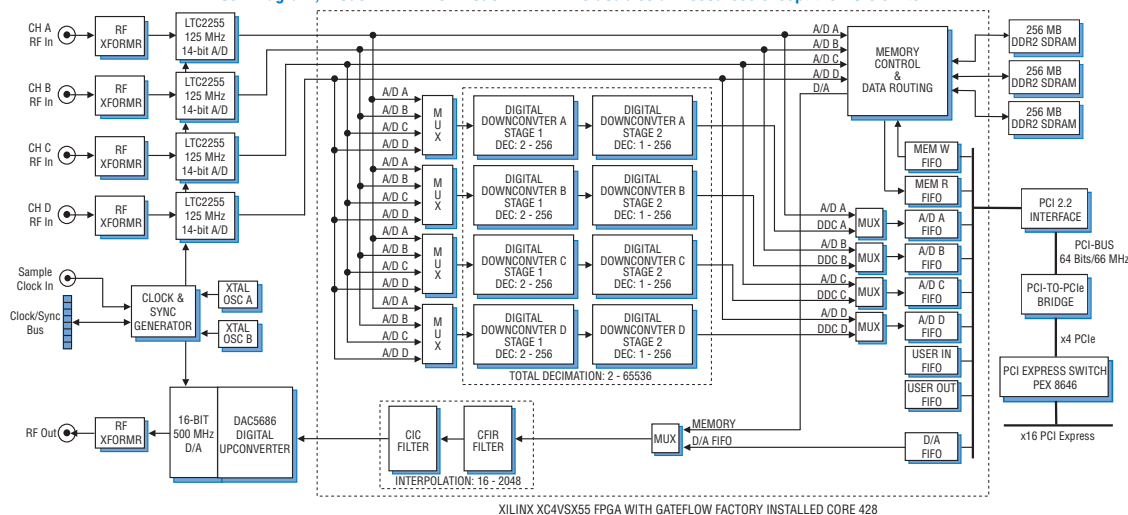
The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7742-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ➤

Block Diagram, Model 7742-428. Model 7742D-428 doubles all resources except the PCIe switch.



XLINX XC4VSX55 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 428

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 7742-428's, or four 7742D-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7742-428 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to each FPGA, as well as one x4 connection to each 64-bit PCI interface.

Ordering Information

Model	Description
7742-428	GateFlow Transceiver with four Multiband DDCs and one Interpolation Filter factory-installed - Full-length x16 PCIe
7742D-428	GateFlow Transceiver with eight Multiband DDCs and two Interpolation Filters factory-installed - Full-length x16 PCIe

Contact Pentek for available options

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal oscillator

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Arrays

Type: Xilinx Virtex-4 XC4VSX55 and Xilinx Virtex-4 XC4VFX60

Memory

DDR2 SDRAM: 768 MB in three banks per SX55/LX100 FPGA (1.5 GB max.)

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port per PCI bus; one x16 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

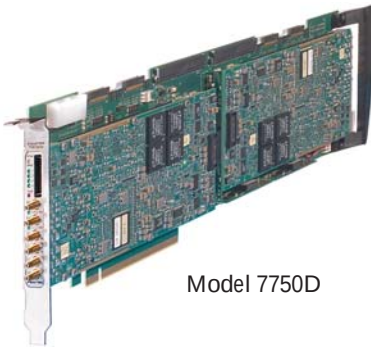
Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

New!

Models 7750, 7750D

Quad/Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x16 PCIe



Model 7750D



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Four or eight 200 MHz 16-bit A/Ds
- Up to 3 GB of DDR2 SDRAM
- Two or Four Xilinx Virtex-5 FPGAs
- Up to 5.12 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- Up to 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7750 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features either four 200 MHz, 16-bit A/Ds (Model 7750) or eight A/Ds (Model 7750D). These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 7750 attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

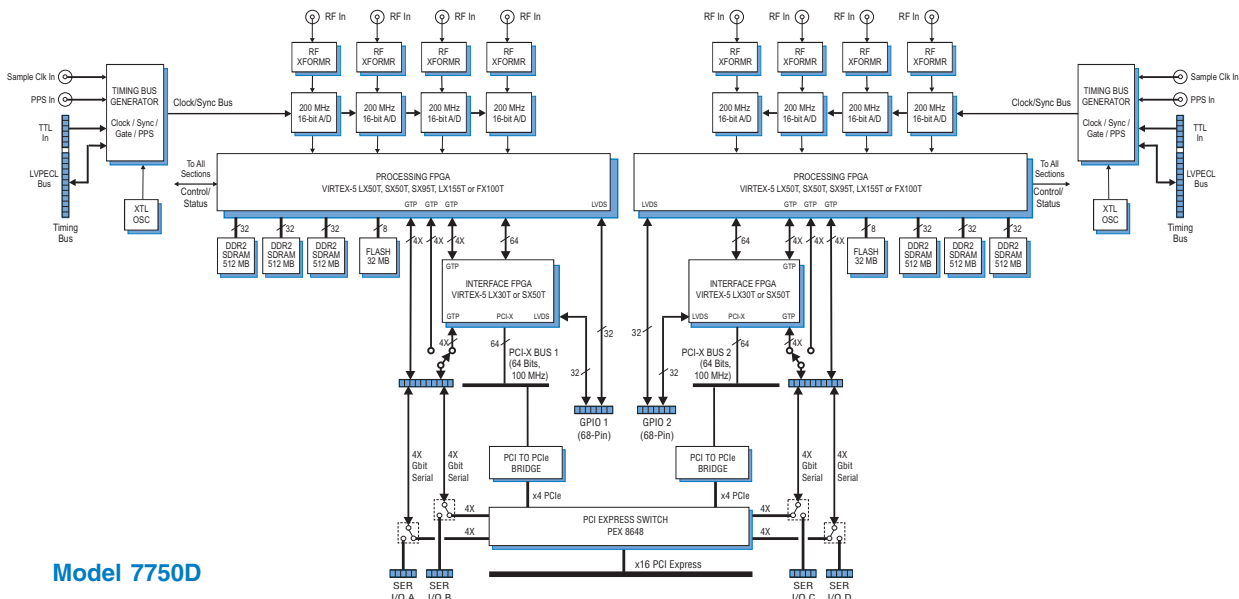
The Model 7750 architecture includes two (Model 7750) or four (Model 7750D) Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

There are two FPGA types on the 7750: processing and interface. The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL/I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, these Models can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express. Implementing the PCI interfaces in this FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to each processing FPGA, and 16 pairs of LVDS connections to each interface FPGA for custom I/O. ➤



Model 7750D

Clocking and Synchronization

The Model 7750 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7750s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to each processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7750 includes a multiple port, 48-lane Gen 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to each FPGA, as well as one x4 connection to each 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX50T (one for 7750, two for 7750D); optional FPGAs include:

XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: Xilinx Virtex-5 XC5VLX30T (one for 7750, two for 7750D); optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to each processing FPGA and 16 pairs to each interface FPGA

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks per processing FPGA (3 GB max.)

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: two x4 ports per FPGA

one x4 port per PCI bus

one x16 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

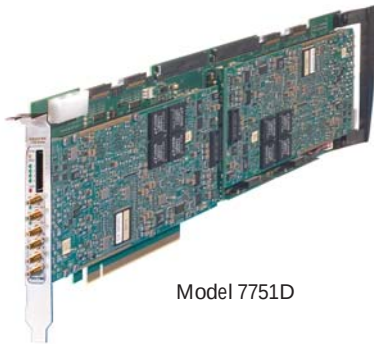
Model	Description
7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length x16 PCIe
7750D	Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length x16 PCIe
Options:	
-104	FPGA I/O through the GPIO connector(s)
-5xx	Gigabit Serial I/O - two full duplex 4X paths (Model 7750) or four full duplex 4X paths (Model 7750D)

Contact Pentek for additional available options.

New!

Models 7751, 7751D

256/512-Channel DDC with 4/8 200 MHz, 16-bit A/Ds - x16 PCIe



Model 7751D



Features

- 256 or 512 DDC channels
- Four or eight 200 MHz 16-bit A/Ds
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Independent tuning for each channel
- DDC decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7751 is a high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features either four 200 MHz 16-bit A/Ds (Model 7751) or eight A/Ds (Model 7751D). Each bank of four A/Ds is supported by a high-performance 256-channel installed DDC IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 7751 attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

Each of the Model 7751 SX95T FPGAs employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the attached four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

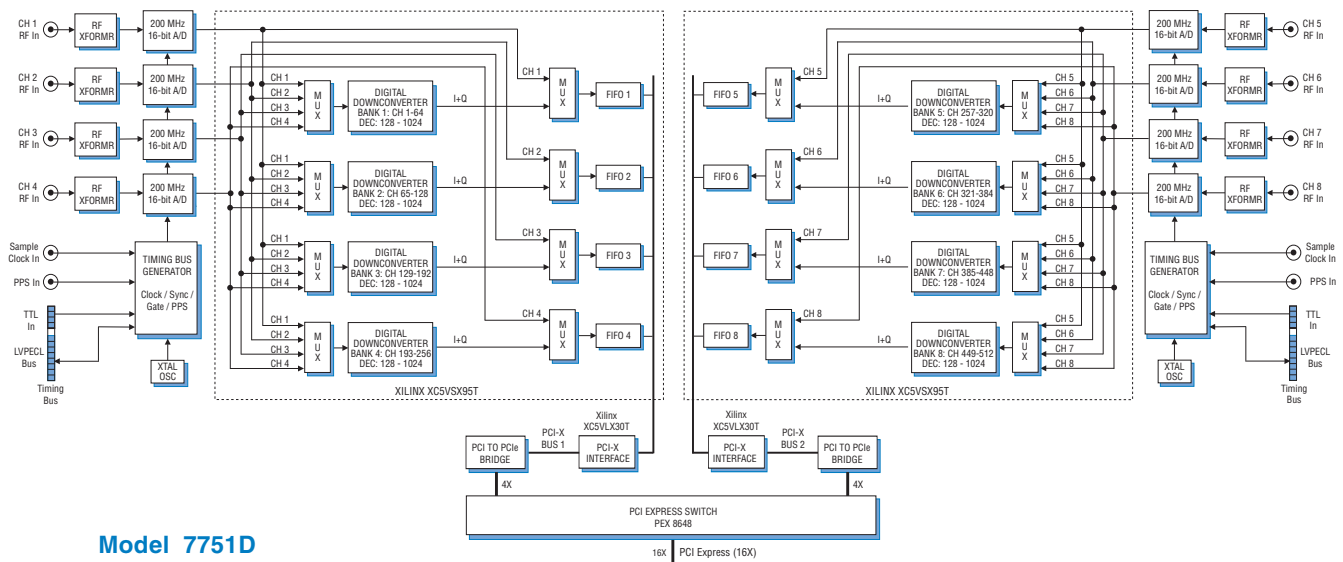
All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Output Multiplexers and FIFOs

Four output MUXs in each SX95T FPGA can be independently switched to deliver either A/D or DDC data into each output FIFO. This allows users to view either wideband A/D data or narrowband DDC data, depending on the application. ➤



Model 7751D

► Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7751 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7751s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7751 includes a multiple port, 48-lane Gen 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with one x4 connection provided to each 64-bit PCI-X interface.

Ordering Information

Model	Description
7751	256-Channel DDC with four 200 MHz, 16-bit A/D - Full-Length x16 PCIe
7751D	512-Channel DDC with eight 200 MHz, 16-bit A/D - Full-Length x16 PCIe

Options:

-731	Two-slot heat sink

Contact Pentek for additional available options.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX95T (one for 7751, two for 7751D) dedicated to digital down-converters and output

Interface FPGA: Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface (one for 7751, two for 7751D)

PCI to PCIe Interface

PCI-X Bus: 64-bits, 133 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port per PCI-X bus one x16 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

New!

Models 7752, 7752D

32/64-Channel DDC with 4/6 200 MHz, 16-bit A/Ds - x16 PCIe



Model 7752D

ReadyFlow
Board Support Package

Features

- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- 32 or 64 channels of DDC in banks of 8 channels
- Independent 32-bit DDC tuning for all channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths from 20 kHz to 10 MHz
- Different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7752 is a high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds (Model 7752) or eight A/Ds (Model 7752D). Each group of four A/Ds is supported by a high-performance 32-channel installed DDC IP Core, and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 7752 attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

Each of the Model 7752 SX95T FPGAs employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four attached A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDCs has an independent 32-bit tuning frequency setting ranging from DC to f_s (f_s is the A/D sample rate).

Decimation and Filtering

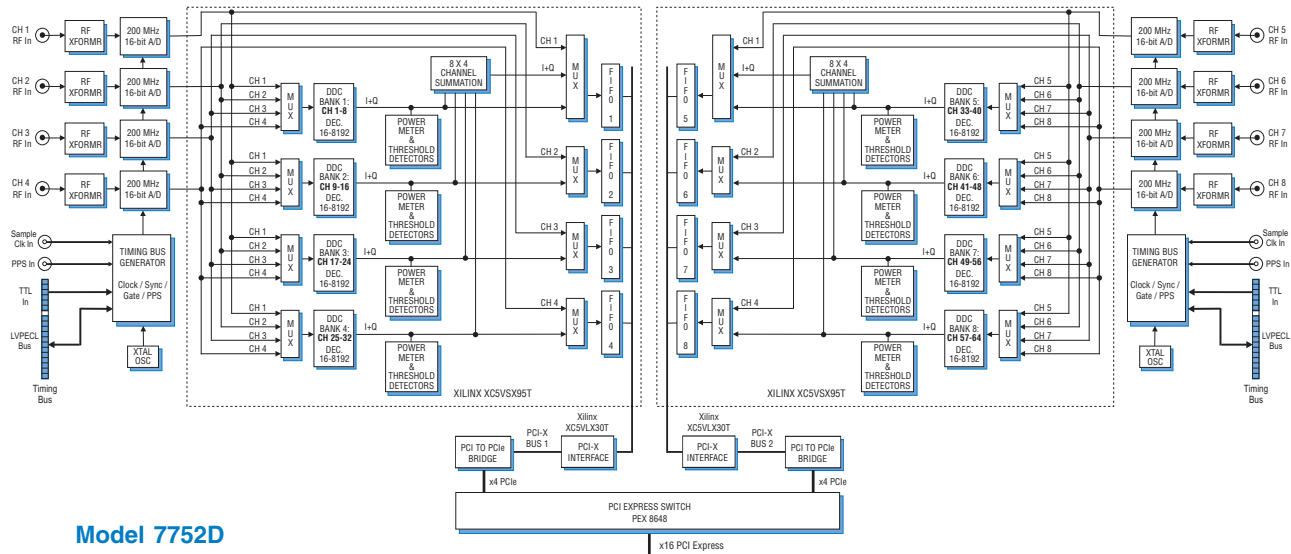
All of the eight channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have a unique decimation setting supporting up to four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. Rejection of adjacent-band components within the 80% bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

The 7752 features up to 64 power meters that continuously measure the individual average power output of each DDC channel. The time constant of the averaging interval for each meter is programmable up to 16K samples. In addition, threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤



Model 7752D

► Output Multiplexers and FIFOs

Four output MUXs in each SX95T FPGA can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7752 architecture includes a flexible timing and synchronization circuit for each group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple modules to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7752s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. For larger systems, many more modules can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7752 includes a multiple port, 48-lane Gen 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with one x4 connection provided to each 64-bit PCI-X interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX95T (one for 7752, two for 7752D) dedicated to digital down-converters and output

Interface FPGA: Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface (one for 7752, two for 7752D)

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port per PCI-X bus
one x16 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

Model	Description
7752	32-Channel DDC with four 200 MHz, 16-bit A/Ds - Full-Length x16 PCIe
7752D	64-Channel DDC with eight 200 MHz, 16-bit A/Ds - Full-Length x16 PCIe

Options:

-731 Two-slot heat sink

Contact Pentek for additional available options.

New!

Models 7753, 7753D

4/8-Ch. DDC, 4/8 200 MHz 16-bit A/Ds, Beamformer - x16 PCIe



Model 7753D

ReadyFlow
Board Support Package

Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- 2 or 4 (Model 7753) and 4 or 8 (Model 7753D) channels of DDC
- Four or eight 200 MHz, 16-bit A/Ds
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization

General Information

Model 7753 is a high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds (Model 7753) or eight A/Ds (Model 7753D). Each group of four A/Ds is supported by a high-performance 4-channel installed DDC and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

The 7753 attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into Xilinx Virtex-5 FPGAs for routing, formatting and signal processing.

DDC Input Selection and Tuning

The Model 7753 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sampling frequency.

Decimation and Filtering

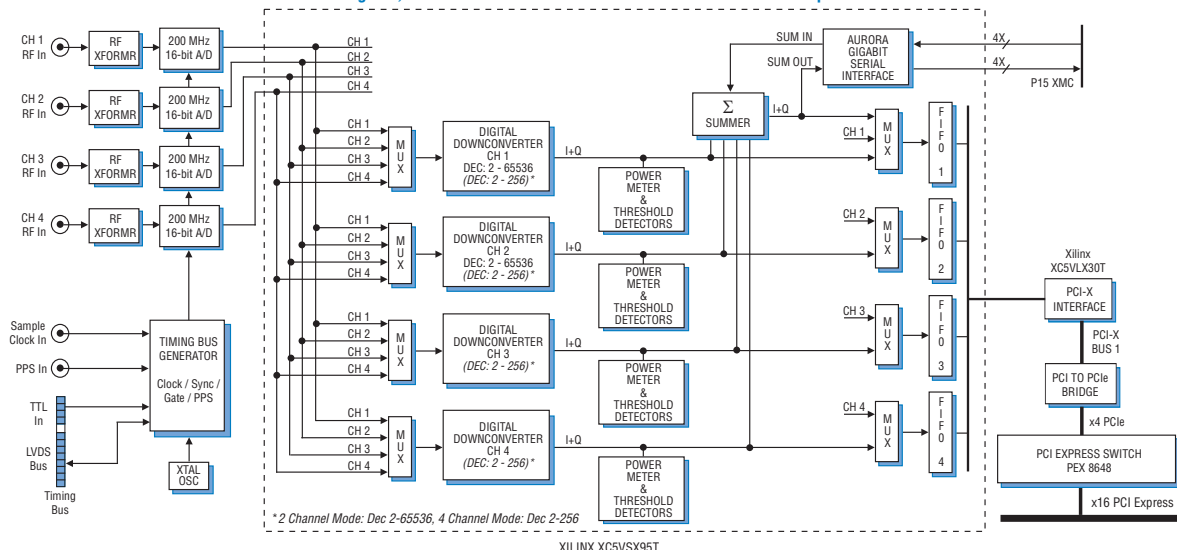
Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N .

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications. ➤

Block Diagram, Model 7753. Model 7753D doubles all resources except the PCIe switch.



XMC Interface

For large systems, multiple 7753's or 7753Ds can be chained together via a built-in Xilinx Aurora interface through the P15 XMC connector.

This link creates a board-to-board summation expansion chain for creating larger multi-channel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

► Beamformer

In addition to the A/Ds and DDCs, these Models include essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable-gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCI-X bus.

For larger systems, multiple Models can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates an x4 sum output stream to the next board through the P15 XMC connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7753 architecture includes a flexible timing and synchronization circuit for each group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

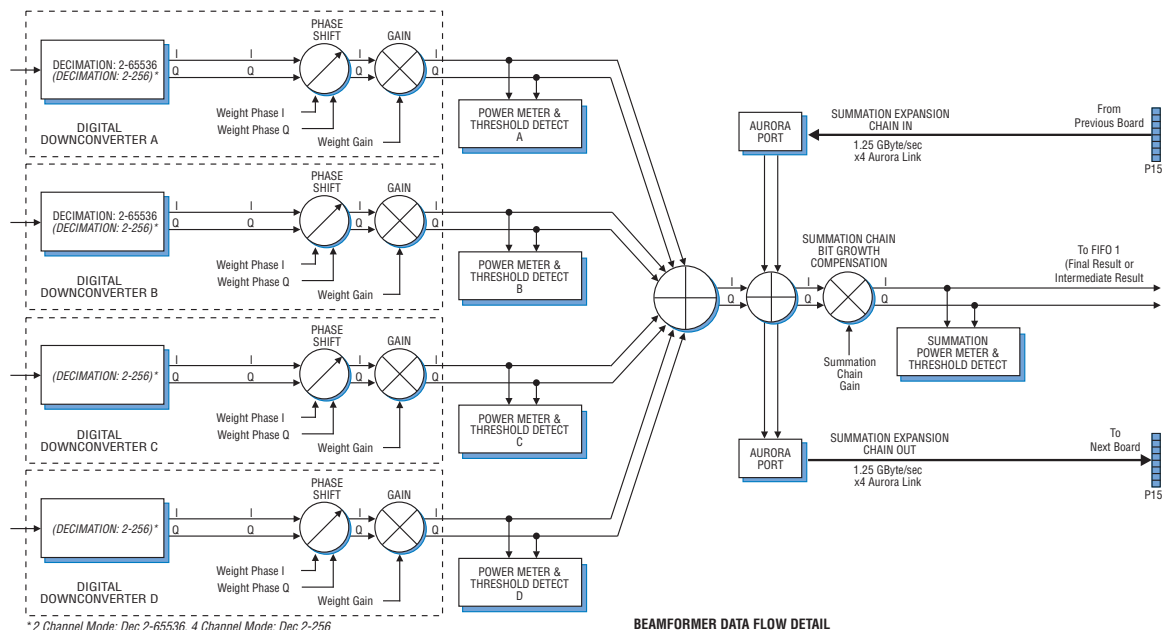
The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7753's can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7753 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with one x4 connection provided to each 64-bit PCI-X interface.



Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillator, external reference or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS, input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Digital Downconverter

Type: IP core for Xilinx Virtex-5

Qty of DDC Channels: 2 or 4 and 4 or 8

Center Frequency Tuning: 4 tuning words, one for each DDC channel

Center Frequency Tuning Range: DC to f_s with 32 bit resolution

NCO SFDR: -120 dBFS

Channel Phase Offset Adjustment: 32-bit resolution

Channel Gain Adjustment: 32-bit resolution

Input Selection for DDC Banks: Any channel can select any of the four A/Ds

Decimation Range (N):

2-Channel Mode: 2 to 65536

4-Channel Mode: 2 to 256

FIR Filter: Default passband $0.8 \cdot f_s / N$ with 0.2 dB passband ripple and 100 dB adjacent channel rejection

FIR Filter Coefficients: 18 bits, user-programmable (default values provided)

Qty FIR Filter Taps: $28 \cdot N / 8$

Output Format: 24 bits I + 24 bits Q

Output Spectrum Modes: Normal or frequency-reversed

Output Spectrum Offset: No offset or offset by one-half the output bandwidth

Beamformer

Summation: Four or eight channels on-board; multiple boards can be summed via Summation Expansion Chain

Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion: 32-bit

Output Multiplexer and FIFO

Qty Output FIFOs: Four or eight

FIFO Source Selection: Independent multiplexer selects DDC output or A/D

PCI to PCIe Interface

PCI-X Bus: 64 bits, 100 MHz and 64 or 32 bits at 33 or 66 MHz

DMA: 4-channel demand-mode and chaining controller per PCI-X bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port per PCI-X bus one x16 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

Model	Description
7753	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - Full-Length x16 PCIe
7753D	8-Channel DDC with eight 200 MHz, 16-bit A/Ds and Beamformers - Full-Length x16 PCIe

Options:

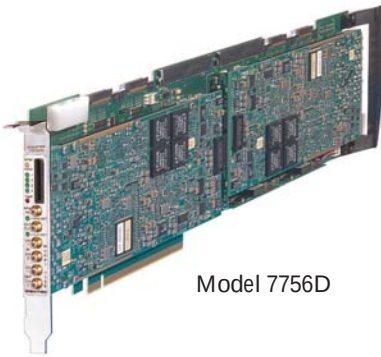
-731 Two-slot heat sink

Contact Pentek for additional available options.

New!

Models 7756, 7756D

Dual/Quad 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - x16 PCIe



Model 7756D



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Two or four 400 MHz, 14-bit A/Ds
- One or two DUCs (Digital Upconverters)
- Two or four 800 MHz, 16-bit D/As
- Up to 2 GB of DDR2 SDRAM
- Two or four Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7756 is a high-speed data converter suitable for connection to HF or IF ports of a communication system. It is available with either two A/Ds, D/As and FPGAs (Model 7756), or four A/Ds, D/As and FPGAs (Model 7756D). It attaches to motherboards with full-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts two or four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

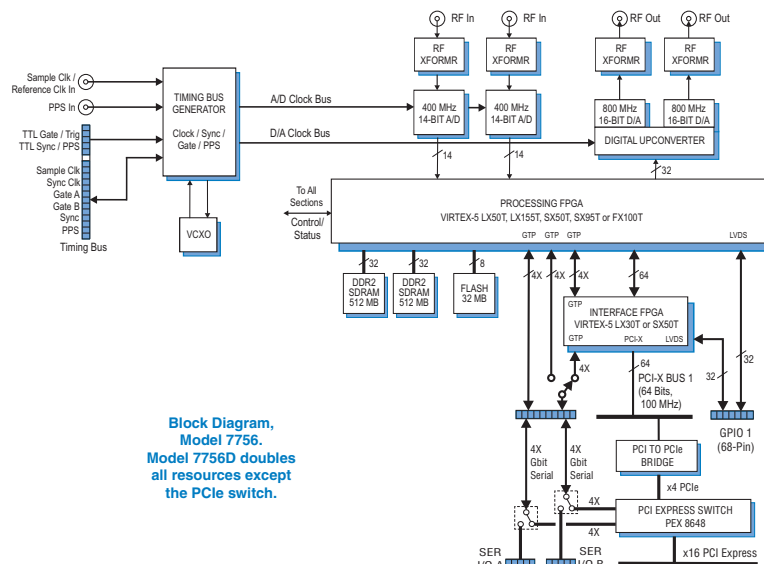
Virtex-5 FPGAs

The architecture includes two or four Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family ➤



Block Diagram,
Model 7756.
Model 7756D doubles
all resources except
the PCIe switch.

PCI Express Interface

The 7756 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports include buffer memory to minimize bottlenecks. Two x4 PCIe connections are provided to each FPGA, as well as one x4 connection to each 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

► part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to each processing FPGA, and 16 pairs of LVDS connections to each interface FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to two slave 7756D's and three slave 7756's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Up to four independent 512 MB banks of DDR2 SDRAM are available to the processing FPGAs. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 400 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: Xilinx Virtex-5

XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to each processing FPGA and 16 pairs to each interface FPGA

Memory

DDR2 SDRAM: Up to 1.0 GB in two banks per processing FPGA (2 GB max.)

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: two x4 ports per FPGA; one x4 port per PCI bus; one x16 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

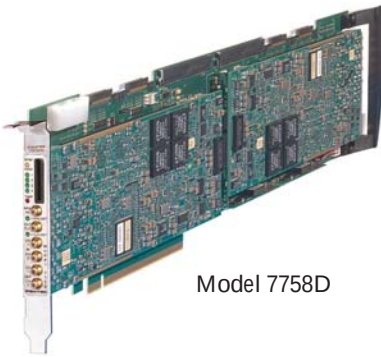
Model	Description
7756	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length x16 PCIe
7756D	Quad 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length x16 PCIe
Options:	
-104	FPGA I/O through the GPIO connector(s)
-5xx	Gigabit serial I/O: two full-duplex 4X paths (Model 7756) or four full duplex-4X paths (Model 7756D)

Contact Pentek for additional available options.

New!

Models 7758, 7758D

Dual/Quad 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - x16 PCIe



Model 7758D



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Two or four 500 MHz, 12-bit A/Ds
- One or two DUCs (Digital Upconverters)
- Two or four 800 MHz, 16-bit D/As
- Up to 2 GB of DDR2 SDRAM
- Two or four Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7758 is a high-speed data converter suitable for connection to HF or IF ports of a communication system. It is available with either two A/Ds, D/As and FPGAs (Model 7758), or four A/Ds, D/As and FPGAs (Model 7758D). It attaches to motherboards with full-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts two or four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5463 12-bit 500 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

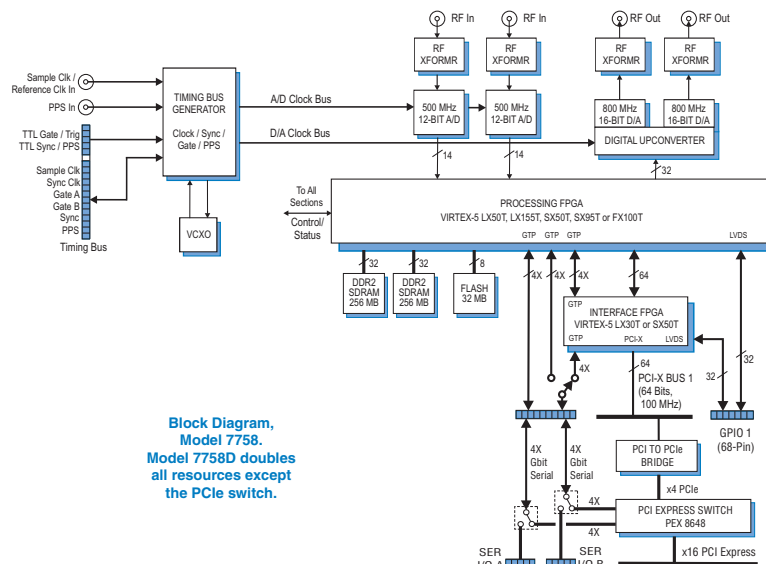
Virtex-5 FPGAs

The architecture includes two or four Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family ➤



Block Diagram,
Model 7758.
Model 7758D doubles
all resources except
the PCIe switch.

PCI Express Interface

The 7758 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports include buffer memory to minimize bottlenecks. Two x4 PCIe connections are provided to each FPGA, as well as one x4 connection to each 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Ordering Information

Model	Description
7758	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length x16 PCIe
7758D	Quad 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length x16 PCIe

Options:

-104	FPGA I/O through the GPIO connector(s)
-140	1 GB DDR2 SDRAM, Model 7758; 2 GB DDR2 SDRAM, Model 7758D
-5xx	Gigabit serial I/O: two full-duplex 4X paths (Model 7758) or four full duplex-4X paths (Model 7758D)

Contact Pentek for additional available options.

► part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to each processing FPGA, and 16 pairs of LVDS connections to each interface FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to two slave 7758D's and three slave 7758's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Two independent 256 MB banks of DDR2 SDRAM are available to the processing FPGA. These can be upgraded to 512 MB banks with option -140. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 500 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: Xilinx Virtex-5

XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to each processing FPGA and 16 pairs to each interface FPGA

Memory

DDR2 SDRAM: Up to 1.0 GB in two banks per processing FPGA (2 GB max.)

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: two x4 ports per FPGA; one x4 port per PCI bus; one x16 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

RADAR & SDR I/O - x8 PCI Express

MODEL	DESCRIPTION
7841	Dual Multiband Transceivers with FPGA - Half-length PCIe
7841-420	Transceiver w. Dual Wideband DDCs and Interpolation Filter - Half-length PCIe
7841-430	Transceiver with 256-Channel Narrowband DDC - Half-length PCIe
7842	Multichannel Transceiver with Virtex-4 FPGAs - Half-length PCIe
7842-428	Transceiver with Four Multiband DDCs and Interpolation Filter - Half-length PCIe
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Half-length PCIe
7851	256-Channel DDC with Four 200 MHz, 16-bit A/Ds - Half-length PCIe
7852	32-Channel DDC with Four 200 MHz, 16-bit A/Ds - Half-length PCIe
7853	4/2-Channel DDC, four 200 MHz 16-bit A/Ds, Beamformer - Half-length PCIe
7856	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe
7858	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe
Cobalt 78620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - Half-length PCIe
Cobalt 78621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - Half-length PCIe
Cobalt 78630	1 GHz A/D and D/A, Virtex-6 FPGA - Half-length PCIe
Cobalt 78650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - Half-length PCIe
Cobalt 78660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - Half-length PCIe
Cobalt 78661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - Half-length PCIe
	Customer Information

[RADAR & SDR I/O - PMC/XMC](#)

[RADAR & SDR I/O - CompactPCI](#)

[RADAR & SDR I/O - PCI](#)

[RADAR & SDR I/O - x16 PCI Express](#)

[RADAR & SDR I/O - 3U VPX](#)

[Click Here for the PRODUCT SELECTOR](#)

Last updated: November 2010



Features

- Complete software radio transceiver solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- Two 125 MHz 14-bit A/Ds
- Input signal bandwidth: 50 MHz
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on P4
- Optional factory-installed IP Cores available

General Information

Model 7841 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters, and is capable of bandwidths to 50 MHz and above. It attaches directly to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

The 7841 features a TI/Graychip GC4016 quad digital downconverter, accepting either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/Ds, FPGA signal processing engine, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By

combining channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter and dual D/A is attached to the FPGA, accepting baseband real or complex data streams with signal bandwidths up to 40 MHz.

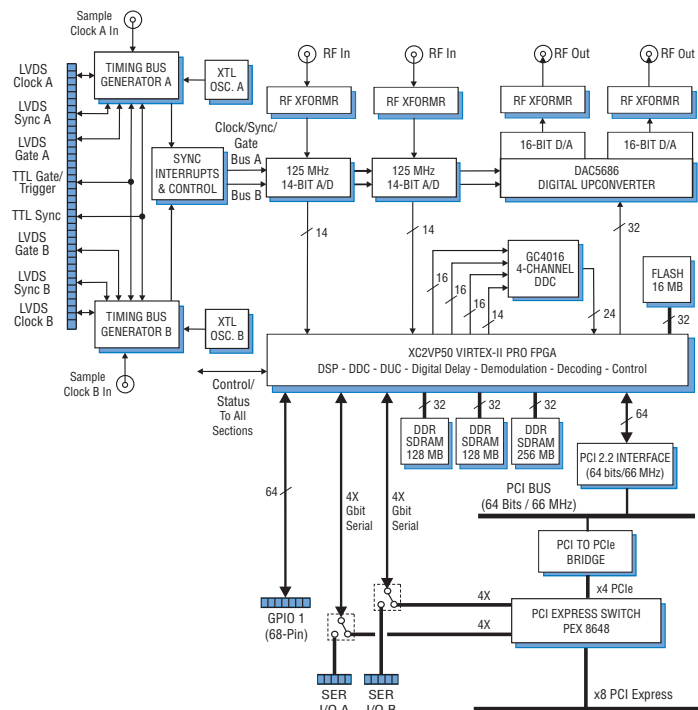
When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGAs

A Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, digital downconverter, digital upconverter and D/A converters.

Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. Option -104 adds 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O. Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the corresponding input and output signals.

Each timing bus includes a clock, sync, and gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the A/Ds, downconverter, upconverter and D/As. Two external reference clocks or two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7841 boards can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available to the FPGA (to 1 GB max.). Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Express Interface

The 7841 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to the FPGA, as well as one x4 connection to the 64-bit PCI interface.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal osc. (2 per A/D)

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

Option -002: -2 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clocks

Type: Female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohm

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro

Option -050: XC2VP50

Option -104: 64 lines (32 pairs)

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

PCIe Ports: two x4 ports to FPGA

one x4 port to PCI bus

one x4 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7841	Dual Multiband Transceiver with FPGA - Half-length x8 PCIe

Options:

-002	Full-scale output: -2 dBm into 50 ohms; 3 dB passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through GPIO connector
-125	125 MHz Bus A and 100 MHz Bus B internal oscillators
-420	Dual wideband DDC and digital interpolation filter cores, factory-installed in FPGA
-430	256-channel narrowband DDC core, factory-installed in FPGA
-5xx	Gigabit Serial I/O - two full duplex 4X paths



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz

General Information

Model 7841-420 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters. This Model attaches directly to motherboards with half-length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital down-converter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGA and to other board resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, this board includes Pentek's GateFlow installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 down-converter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

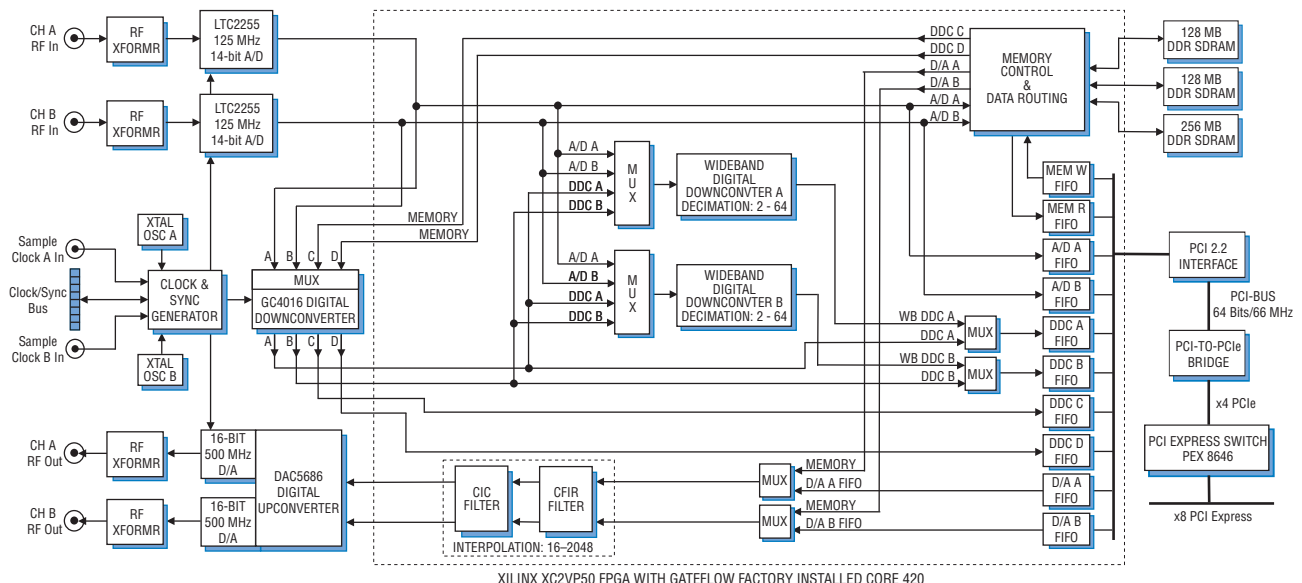
Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of the Model 7841 are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7841-420's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7841-420 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with a x4 connection provided to the 64-bit PCI interface.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI bus, one x8 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7841-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - Half-length x8 PCIe

Contact Pentek for available options



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- GateFlow Core 430 with 256 channels of narrowband digital downconverters factory-installed
- 256 programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

General Information

Model 7841-430 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters. This Model attaches directly to motherboards with half-length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital down-converter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGA and to other board resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7841-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC

filter coefficient sets are included with the core for all possible decimation settings.

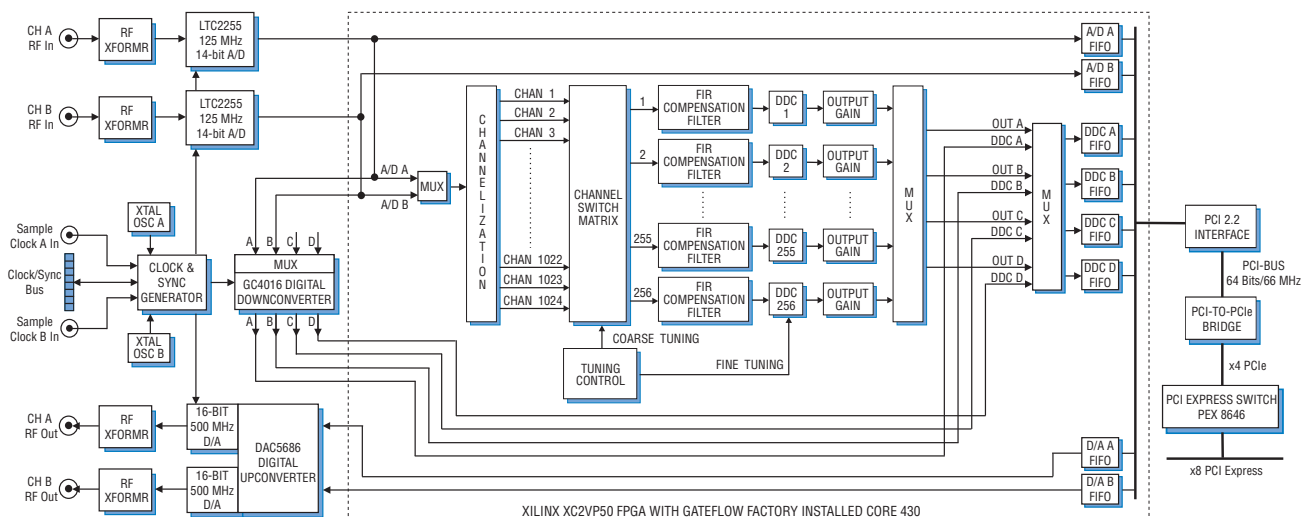
Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2^{32}
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in this Model. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7841-430's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7841-430 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with a x4 connection provided to the 64-bit PCI interface.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI bus, one x8 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7841-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - Half-length x8 PCIe

Contact Pentek for available options



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- Switched fabric support
- 125 MHz 14-bit A/Ds
- Digital upconverters
- 500 MHz 16-bit D/As
- Up to 768 MB of DDR2 SDRAM
- Xilinx Virtex-4 FPGAs
- LVDS clock/sync bus for multimodule synchronization
- Optional factory-installed IP Cores available

General Information

Model 7842 is a multichannel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds with one upconverter and D/A converter. It attaches to mother-boards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computers.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into a Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

The 7842 features a TI DAC5686 digital upconverter (DUC) and D/A. It accepts a baseband real or complex data stream from its attached FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, the DAC5686 interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs up to 320 MHz to the 16-bit D/A converter. If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

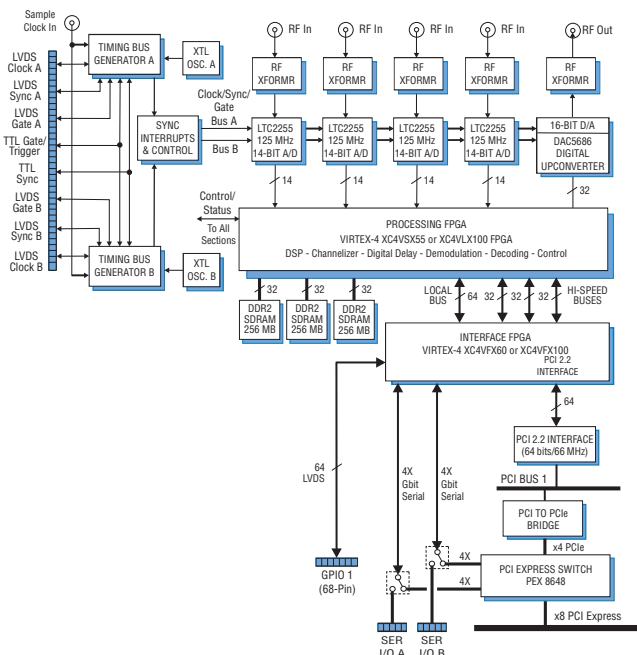
The 7842 architecture includes two Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can include their own custom IP, and integrate it with factory-shipped functions using a Pentek GateFlow FPGA Design Kit.

The Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for implementing functions such as demodulation/modulation, digital delay and channelization. For applications requiring more FPGA logic cells, the Model 7842 can be optionally configured with XC4VLX100 in place of each XC2VSX55 for up to 221,184 logic cells.

A Virtex-4 XC4VFX60 Interface FPGA provides board interfaces including PCI and serial I/O. The interface FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. The Model 7842 can be optionally configured with XC4VFX100 in place of each FX60.

Option -104 installs a GPIO connector with 32 pairs of LVDS connections to the XC4VFX60/100 Interface FPGA for custom I/O. ➤



PCI Express Interface

The 7842 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes.

The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two optional x4 PCIe connections to the SX55/LX100 FPGA, and one x4 connection to the 64-bit PCI interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Ordering Information

Model Description

7842 Multichannel Transceiver with four A/Ds, one D/A and Virtex-4 FPGAs - Half-length x8 PCIe

Options:

-100 XC4VFX100 replaces XC4VFX60
 -104 FPGA I/O through GPIO connector
 -110 XC4VLX100 replaces XC4VSX55
 -428 Four multiband DDCs and interpolation filter, factory-installed core in the processing FPGA
 -5xx Gigabit Serial I/O - two full duplex 4X paths

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the A/Ds, upconverter and D/A. Internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, each LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7842s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the SX55 or LX100 FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal osc.

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms (other options available)

3 dB Passband: 60 kHz to 300 MHz (other options available)

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-4 XC4VSX55 & Xilinx Virtex-4 XC4VFX60

Option -100: XC4VFX100 replaces XC4VFX60

Option -110: XC4VLX100 replaces XC4VSX55

Custom I/O

Option -104: Adds GPIO connector with 32 lines to the XC4VFX60/100 FPGA

Memory

DDR2 SDRAM: 768 MB in three banks to SX55/LX100 FPGA

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

Ports: one x4 port to PCI bus
 one x8 port to PCIe motherboard;
 two optional x4 ports to Interface FPGA for other gigabit protocols

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- GateFlow IP Core 428, with four high-performance multiband DDCs and one Interpolation Filter, factory-installed
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4

General Information

Model 7842-428 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features four A/D and one D/A converters. This Model attaches directly to motherboards with half-length PCIe (PCI Express) interface slots for installation in various PCs, blade servers and computer systems.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other module resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating FIR filters. Each filter is capable of any deci-

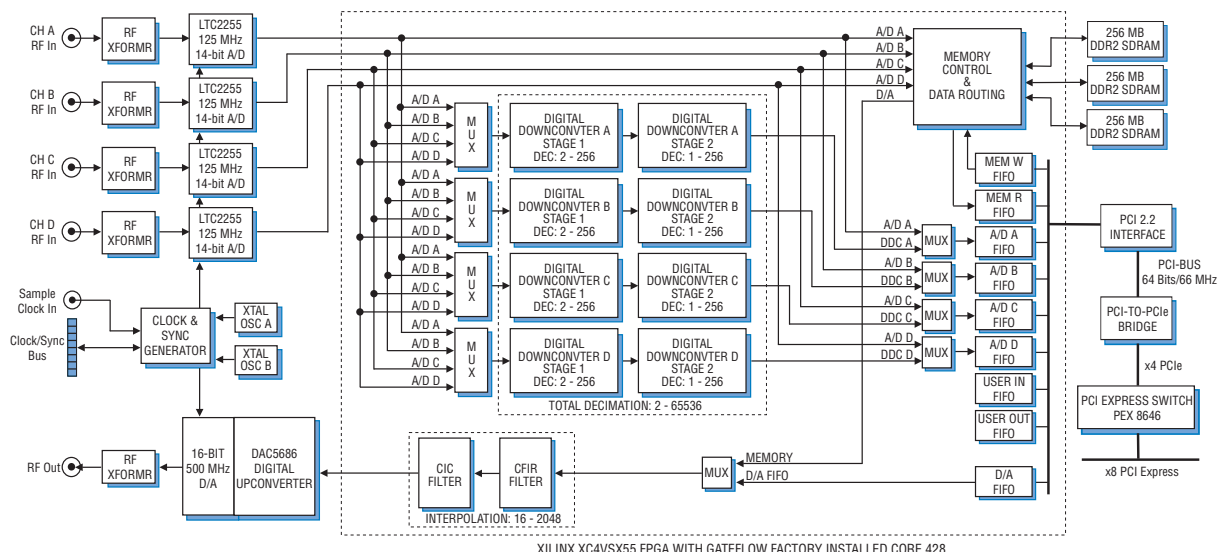
mation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7842-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ➤



► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 7842-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7842-428 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with a x4 connection provided to the 64-bit PCI interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal oscillator

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Arrays

Type: Xilinx Virtex-4 XC4VSX55 and Xilinx Virtex-4 XC4VFX60

Memory

DDR2 SDRAM: 768 MB in three banks of 256 MB each

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI bus, one x4 port to PCIe motherboard

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7842-428	GateFlow Transceiver with four Multiband DDCs and one Interpolation Filter factory-installed - Half-length x8 PCIe

Contact Pentek for available options

New!

Model 7850

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x8 PCIe



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- Up to 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7850 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds. These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 7850 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The Model 7850 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

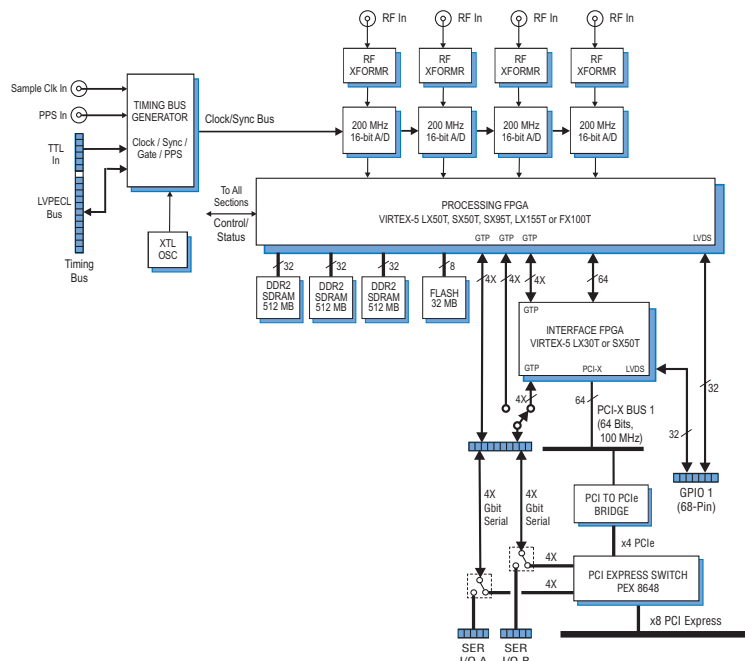
There are two FPGA types on the 7850: processing and interface. The pro-

cessing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7150 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express. Implementing the PCI interfaces in this FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O. ➤



Clocking and Synchronization

The Model 7850 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7850s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7850 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to the processing FPGA, as well as one x4 connection to the 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5

XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: Xilinx Virtex-5

XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

PCIe Ports: two x4 ports to processing FPGA; one can be alternately routed to interface FPGA

one x4 port to PCI bus

one x8 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Half-length x8 PCIe
Options:	
-104	FPGA I/O through the GPIO connector(s)
-5xx	Gigabit Serial I/O - two full duplex 4X paths

Contact Pentek for additional available options.



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- 256 DDC channels
- Four 200 MHz 16-bit A/Ds
- Independent tuning for each channel
- DDC decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7851 is a high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds. The A/D converters are supported by a high-performance 256-channel installed DDC (digital down-converter) IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 7851 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 7851 SX95T FPGA employs an advanced FPGA-based digital down-converter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the attached four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved

including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

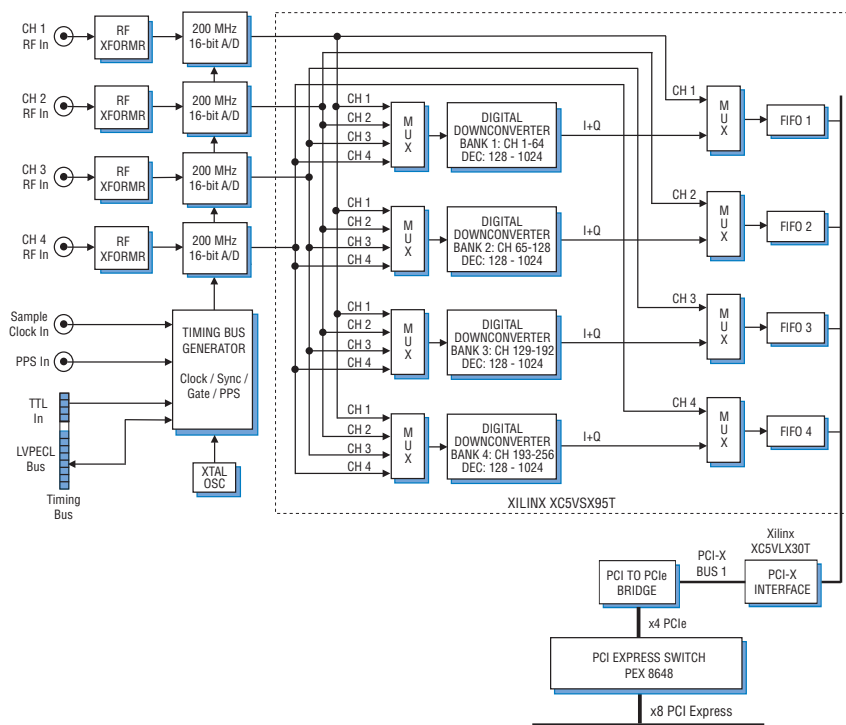
Each of the DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N . Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank. ➤



► Output Multiplexers and FIFOs

Four output MUXs in the SX95T FPGA can be independently switched to deliver either A/D or DDC data into each output FIFO. This allows users to view either wideband A/D data or narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7851 architecture includes a flexible timing and synchronization circuit for the bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connectors allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7851s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7851 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with a x4 connection provided to the 64-bit PCI-X interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX95T dedicated to digital downconverters and output

Interface FPGA: Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface

PCI to PCIe Interface

PCI-X Bus: 64-bits, 133 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI-X bus
one x8 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7851	256-Channel DDC with four 200 MHz, 16-bit A/D - Half-length x8 PCIe

Options:

-731	Two-slot heat sink

Contact Pentek for additional available options.

New!

Model 7852

32-Channel DDC with Four 200 MHz, 16-bit A/Ds - x8 PCIe



ReadyFlow
Board Support Package

Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- 32 channels of DDC in banks of 8 channels
- Independent 32-bit DDC tuning for all channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths from 20 kHz to 10 MHz
- Different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7852 is a high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds. The A/Ds are supported by a high-performance 32-channel installed DDC (digital downconverter) IP Core, and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 7852 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 7852 SX95T FPGA employs an advanced FPGA-based digital down-converter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four attached A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDCs has an independent 32-bit tuning frequency setting ranging from DC to f_s (f_s is the A/D sample rate).

Decimation and Filtering

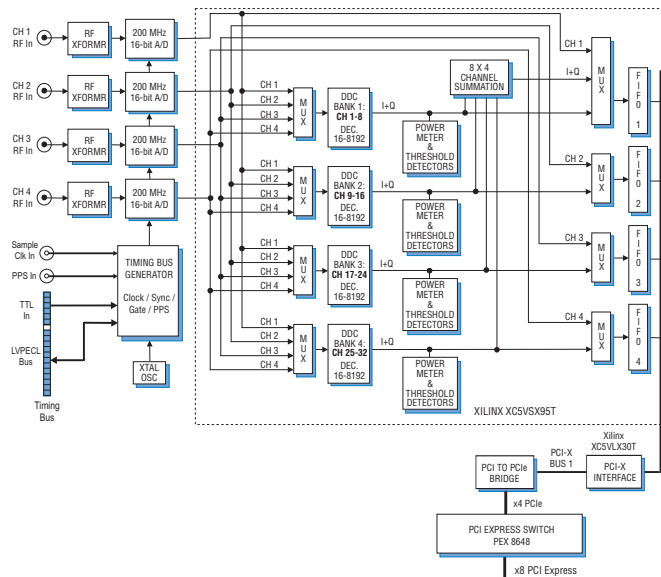
All of the eight channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have a unique decimation setting supporting up to four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. Rejection of adjacent-band components within the 80% bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

The 7852 features 32 power meters that continuously measure the individual average power output of each DDC channel. The time constant of the averaging interval for each meter is programmable up to 16 kilosamples. In addition, threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤



► Output Multiplexers and FIFOs

Four output MUXs in the SX95T FPGA can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7852 architecture includes a flexible timing and synchronization circuit for the group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7852s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. For larger systems, many more modules can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7852 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with one x4 connection provided to the 64-bit PCI-X interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX95T dedicated to digital downconverters and output

Interface FPGA: Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI-X bus
one x8 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7852	32-Channel DDC with four 200 MHz, 16-bit A/Ds - Half-length x8 PCIe

Options:

-731	Two-slot heat sink

Contact Pentek for additional available options.

New!

Model 7853

4/2-Ch. DDC, four 200 MHz 16-bit A/Ds, Beamformer - x8 PCIe



Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- Four 200 MHz, 16-bit A/Ds
- 2 or 4 Channels of DDC
- PCI Express 2.0 (Gen. 2) interface up to x8 wide
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization

General Information

Model 7853 is a high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel installed DDC (digital down-converter) and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

The 7853 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 7853 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency.

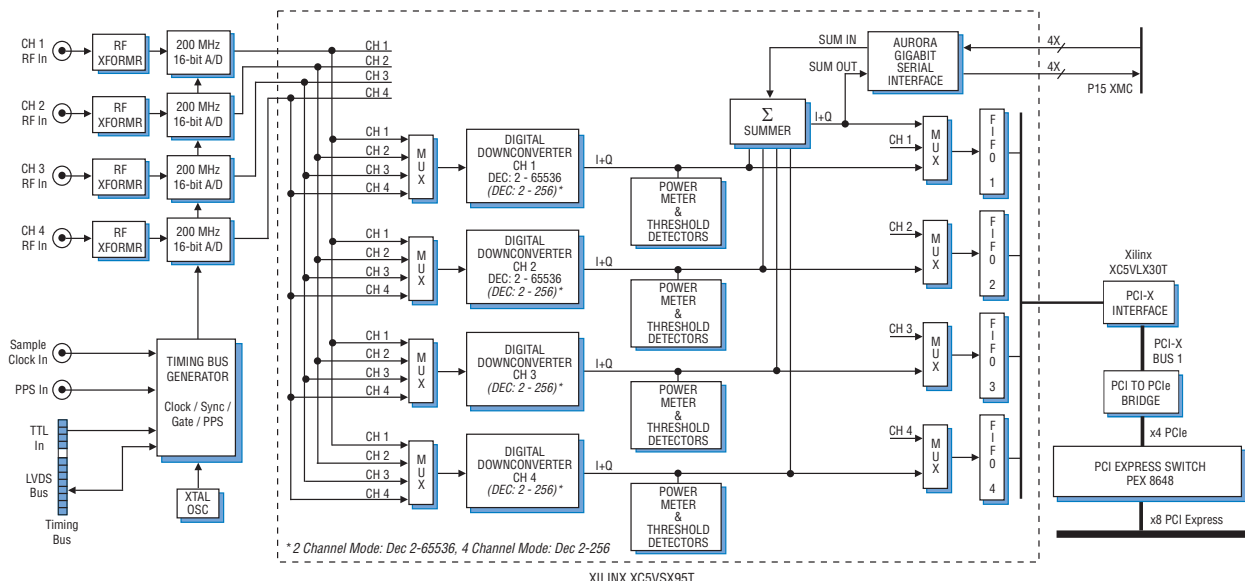
Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N .

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications. ➤



XMC Interface

For large systems, multiple 7853's can be chained together via a built-in Xilinx Aurora interface through the P15 XMC connector.

This link creates a board-to-board summation expansion chain for creating larger multi-channel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

► Beamformer

In addition to the A/Ds and DDCs, these Models include essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable-gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCI-X bus.

For larger systems, multiple Models can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates an x4 sum output stream to the next board through the P15 XMC connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7853 architecture includes a flexible timing and synchronization circuit for the group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

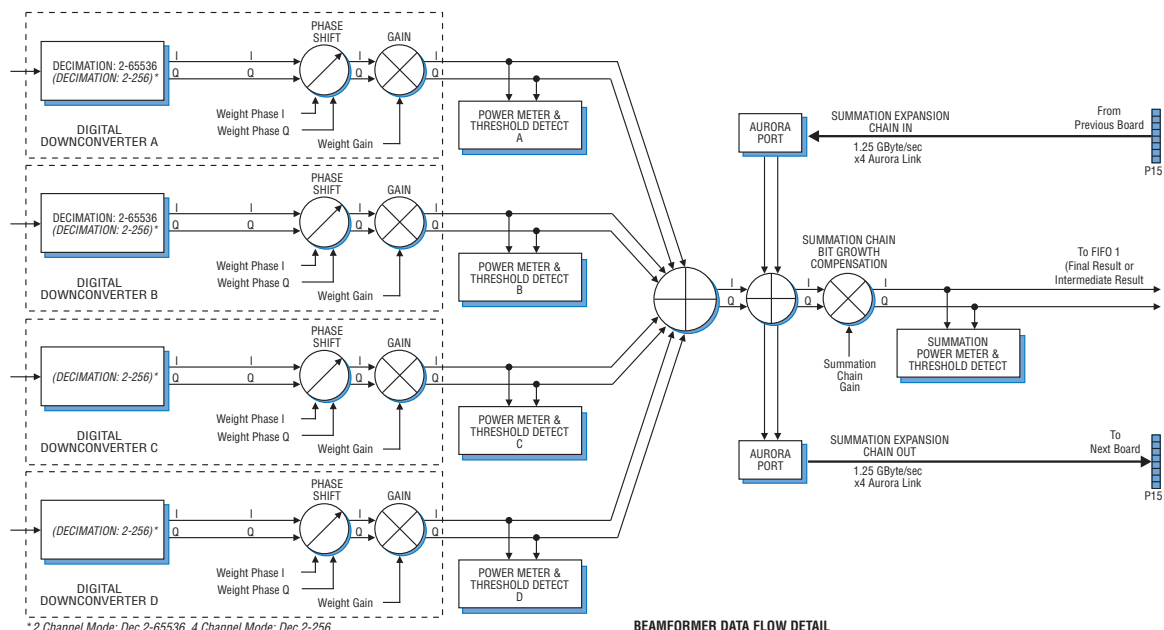
The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7853's can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7853 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with one x4 connection provided to the 64-bit PCI-X interface.



Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillator, external reference or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS, input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Digital Downconverter

Type: IP core for Xilinx Virtex-5

Qty of DDC Channels: 2 or 4

Center Frequency Tuning: 4 tuning words, one for each DDC channel

Center Frequency Tuning Range: DC to f_s with 32 bit resolution

NCO SFDR: -120 dBFS

Channel Phase Offset Adjustment: 32-bit resolution

Channel Gain Adjustment: 32-bit resolution

Input Selection for DDC Banks: Any channel can select any of the four A/Ds

Decimation Range (N):

2-Channel Mode: 2 to 65536

4-Channel Mode: 2 to 256

FIR Filter: Default passband $0.8 \cdot f_s / N$ with 0.2 dB passband ripple and 100 dB adjacent channel rejection

FIR Filter Coefficients: 18 bits, user-programmable (default values provided)

Qty FIR Filter Taps: $28 \cdot N / 8$

Output Format: 24 bits I + 24 bits Q

Output Spectrum Modes: Normal or frequency-reversed

Output Spectrum Offset: No offset or offset by one-half the output bandwidth

Beamformer

Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain

Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion: 32-bit

Output Multiplexer and FIFO

Qty Output FIFOs: Four

FIFO Source Selection: Independent multiplexer selects DDC output or A/D

PCI to PCIe Interface

PCI-X Bus: 64 bits, 100 MHz and 64 or 32 bits at 33 or 66 MHz

DMA: 4-channel demand-mode and chaining controller

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI-X bus one x8 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7853	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - Half-length x8 PCIe

Options:

-731	Two-slot heat sink

Contact Pentek for additional available options.

New!

Model 7856

Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - x8 PCIe



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- Two 400 MHz, 14-bit A/Ds
- One DUC (Digital Upconverter)
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7856 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communication system. It includes two 400 MHz A/Ds, 800 MHz D/As and Virtex-5 FPGAs.

The 7856 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TIADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the processing FPGA for signal processing, capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC provides interpolation factors of 2x, 4x and 8x.

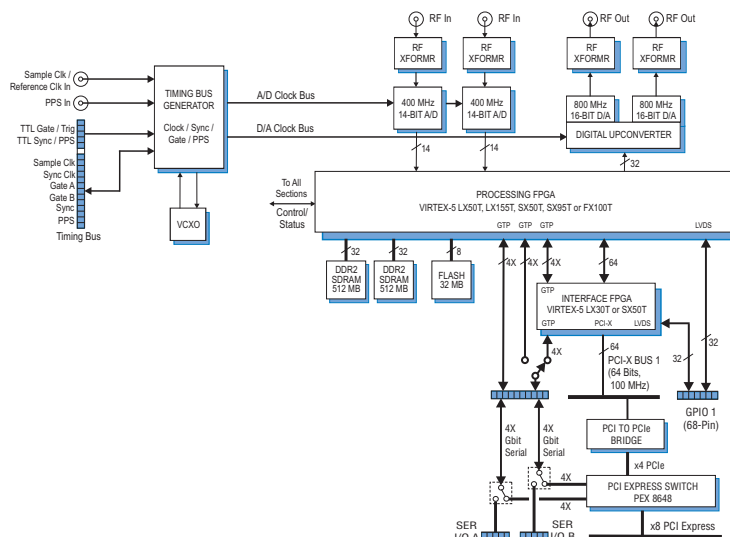
Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family ►



PCI Express Interface

The 7856 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports include buffer memory to minimize bottlenecks. Two x4 PCIe connections are provided to the FPGA, as well as one x4 connection to the 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Ordering Information

Model	Description
7856	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length x8 PCIe

Options:

-104	FPGA I/O through the GPIO connector(s)
-5xx	Gigabit serial I/O: two full-duplex 4X paths

Contact Pentek for additional available options.

► part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 7856's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGAs. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 400 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: Xilinx Virtex-5

XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Xilinx Virtex-5

XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to each processing FPGA and 16 pairs to each interface FPGA

Memory

DDR2 SDRAM: Up to 1.0 GB in two banks to processing FPGA

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

PCIe Ports: two x4 ports to FPGA; one x4 port to PCI bus; one x8 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

New!

Model 7858

Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - x8 PCIe



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- Two 500 MHz, 12-bit A/Ds
- One DUC (Digital Upconverter)
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7858 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communication system. It includes two 500 MHz A/Ds, 800 MHz D/As and Virtex-5 FPGAs.

The 7858 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TIADS5463 12-bit 500 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the processing FPGA for signal processing, capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TIDAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC provides interpolation factors of 2x, 4x and 8x.

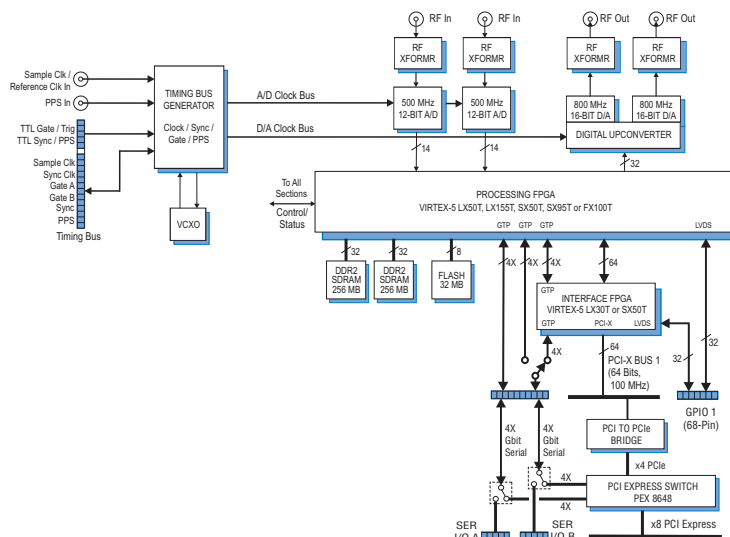
Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface ➤



PCI Express Interface

The 7858 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports include buffer memory to minimize bottlenecks. Two x4 PCIe connections are provided to the FPGA, as well as one x4 connection to the 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Ordering Information

Model	Description
7858	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length x8 PCIe
Options:	
-104	FPGA I/O through the GPIO connector
-140	1 GB DDR2 SDRAM
-5xx	Gigabit serial I/O: two full-duplex 4X paths

Contact Pentek for additional available options.

► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 7858's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Two independent 256 MB banks of DDR2 SDRAM are available to the processing FPGA. These can be upgraded to 512 MB banks with option -140. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 500 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: Xilinx Virtex-5

XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Xilinx Virtex-5

XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to each processing FPGA and 16 pairs to each interface FPGA

Memory

DDR2 SDRAM: Up to 1.0 GB in two banks to processing FPGA

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

PCIe Ports: two x4 ports to FPGA; one x4 port to PCI bus; one x8 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

New!

Model 78620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - x8 PCIe



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User-configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78620 is the first member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78620 includes general purpose and gigabit serial card edge connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchro-

nization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

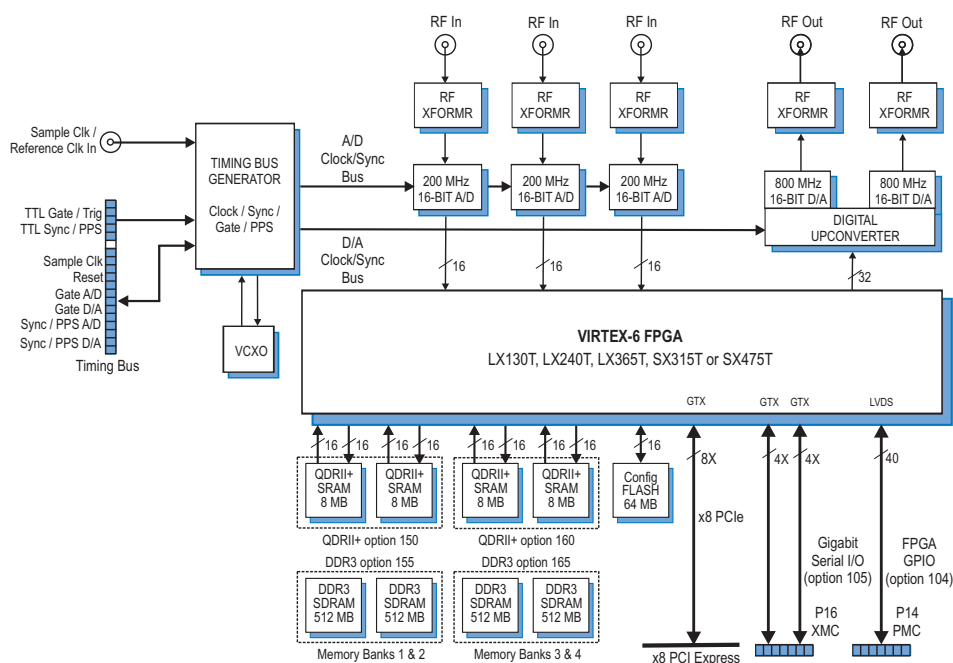
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤



A/D Acquisition IP Modules

The 78620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

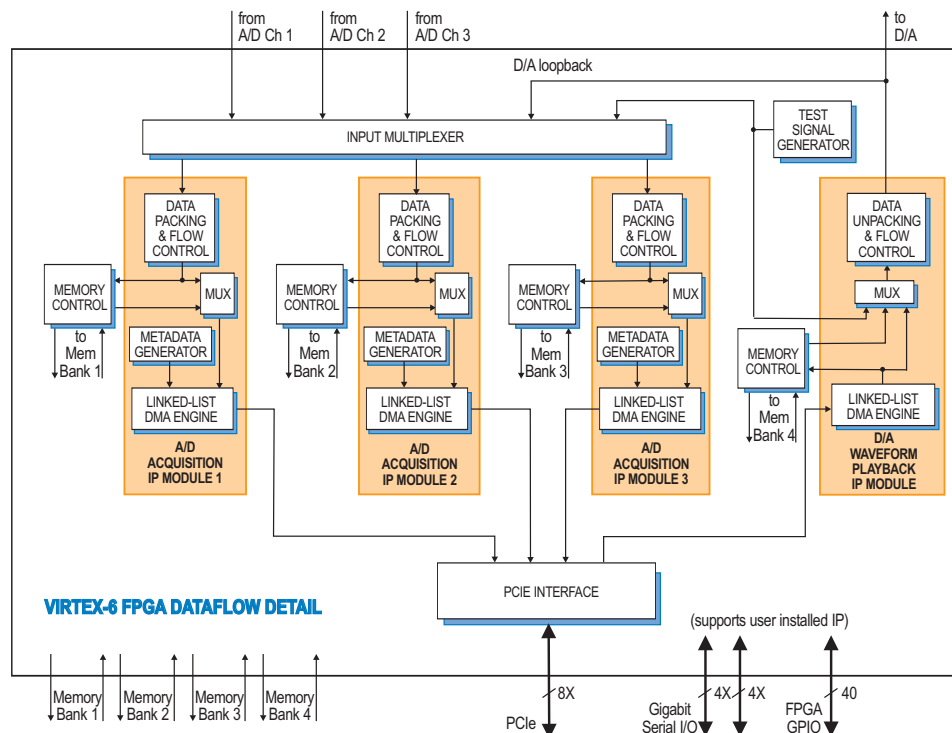
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



► board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78620 3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - PCIe

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

Rev. 0702

PENTEK

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New!

Model 78621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

General Information

Model 78621 is a member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78621 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to

the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

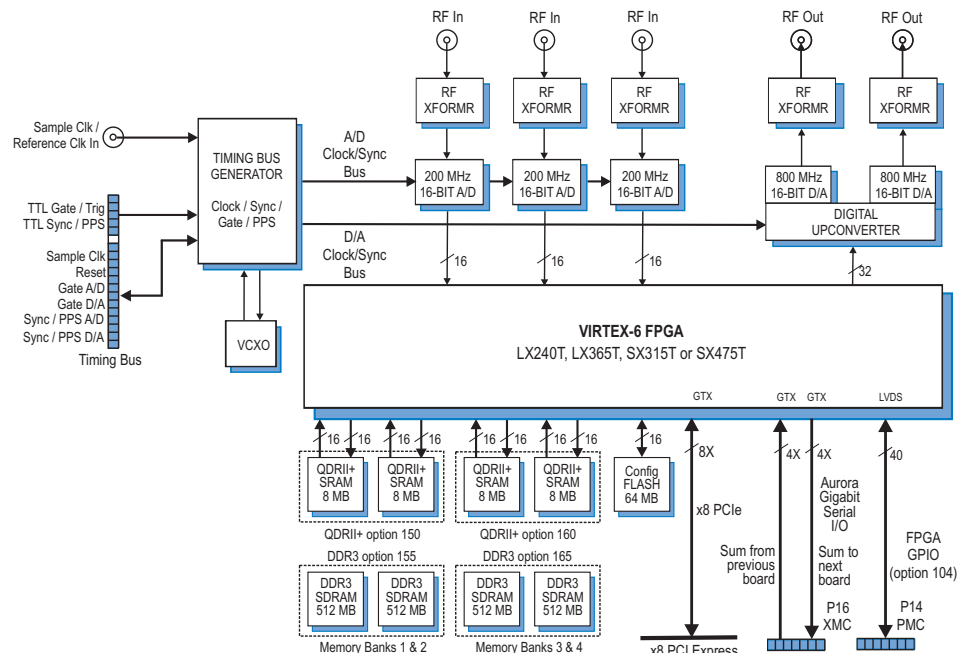
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- LVDS connections to the Virtex-6 FPGA for custom I/O



A/D Acquisition IP Modules

The 78621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to

f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Beamformer IP Core

In addition to the DDCs, the 78621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average

power level of any DDC core falls below or exceeds a programmable threshold.

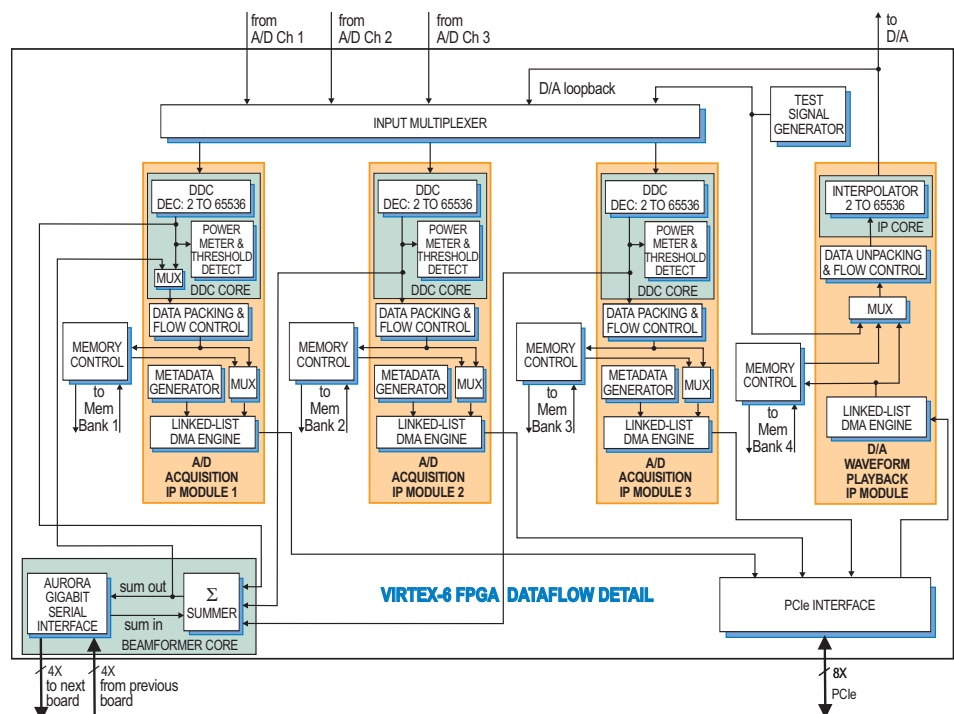
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 78621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



► A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TIDAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alter-

nate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board. ►

► Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Digital Downconverters

Quantity: Three channels

Decimation Range: 2 to 65,536 in integer steps

LO Tuning Freq. Resolution: 32 bits, 0 to Fs

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 2 Pi radians

FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation

Resolution: 16 bits

Digital Interpolator

Interpolation Range: 2x to 65,536 in integer steps

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or a 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78621 3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 78630

1 GHz A/D and D/A, Virtex-6 FPGA - x8 PCIe



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78630 is a member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking

and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

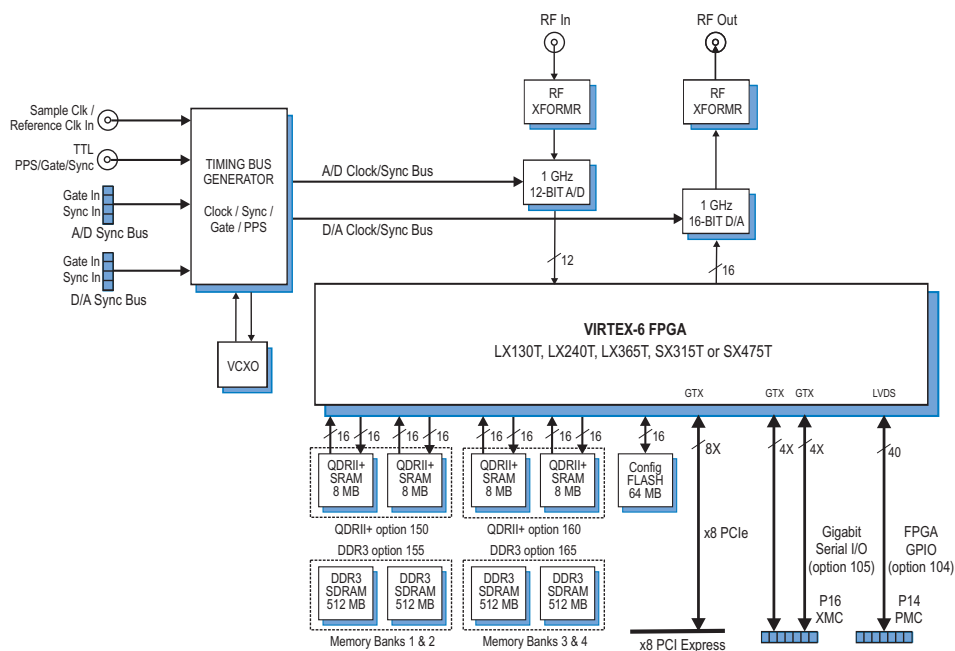
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. ➤



A/D Acquisition IP Module

The 78630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

D/A Converter Stage

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided

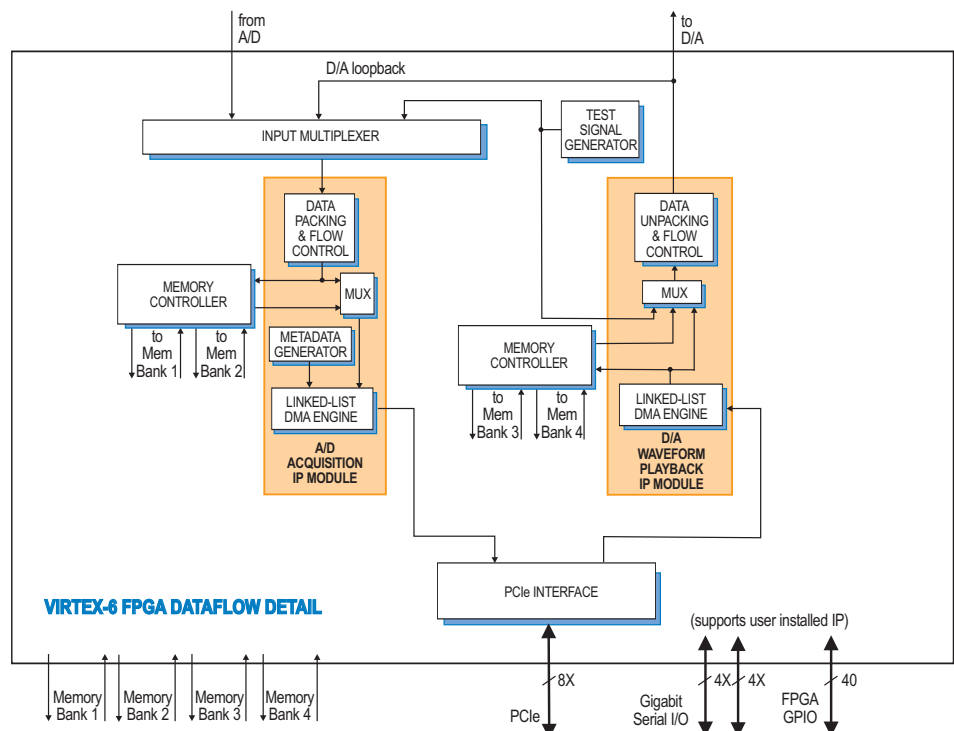
by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Two front panel 7-pin LVPECL Sync connectors allow multiple boards to be synchronized. One connector for the A/D and one for the D/A each provide sync and gate signals.

Memory Resources

The 78630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



► PCI Express Interface

The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts sample clock or a 5 or 10 MHz system reference

Timing Bus: 7-pin connectors, LVPECL bus for sync and gate, one A/D connector and one D/A connector

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78630 1 GHz A/D and D/A,
Virtex-6 FPGA - x8 PCIe

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 78650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - x8 PCIe



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 2) interface up to x8 wide
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78650 is a member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78650 includes optional general-purpose and gigabit serial card connectors for application specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+

memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

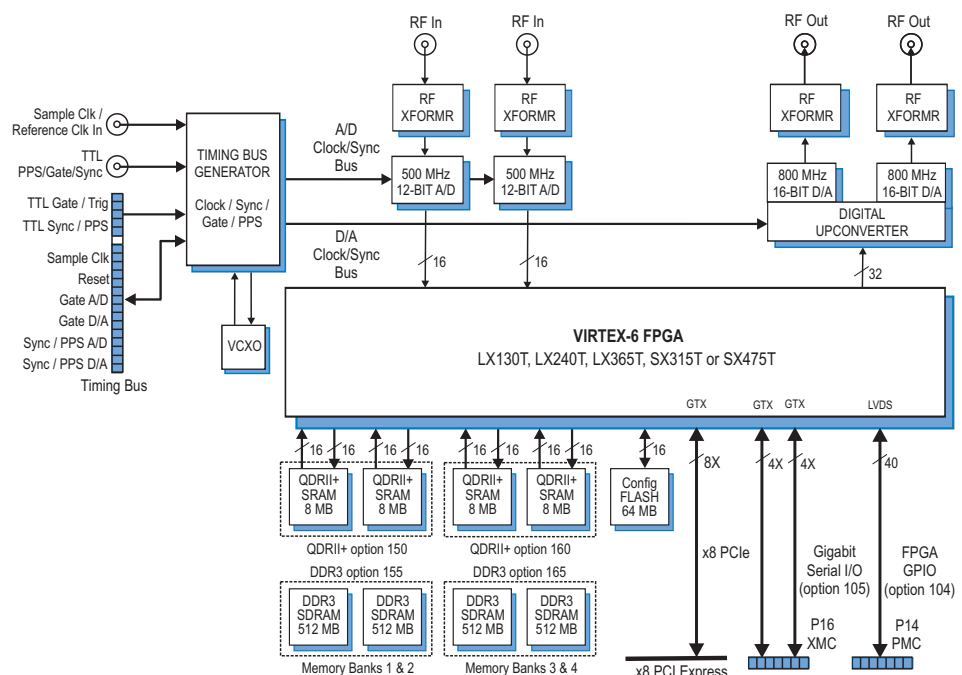
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. ➤



A/D Acquisition IP Modules

The 78650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

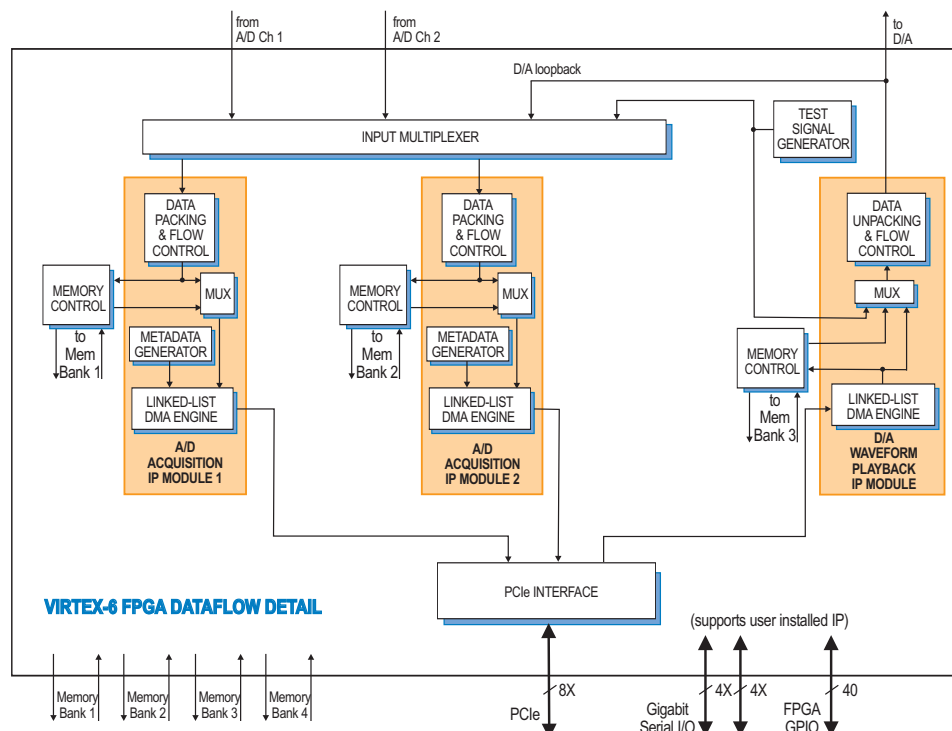
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



► board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

A/D Converters (option 014)

Type: Texas Instruments ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz, max.

Output IF: DC to 400 MHz, max.

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz, max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 800 MHz sample clock or a 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs the XMC P16 connector with two 4X serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78650 Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As with Virtex-6 FPGA - x8 PCIe

Options:

-014 400 MHz, 14-bit A/Ds
-062 XC6VLX240T
-063 XC6VLX365T
-064 XC6VSX315T
-065 XC6VSX475T
-104 LVDS FPGA I/O through P14 connector
-105 Gigabit serial FPGA I/O through P16 connector
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 78660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - x8 PCIe



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User-configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78660 is the second member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal

generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

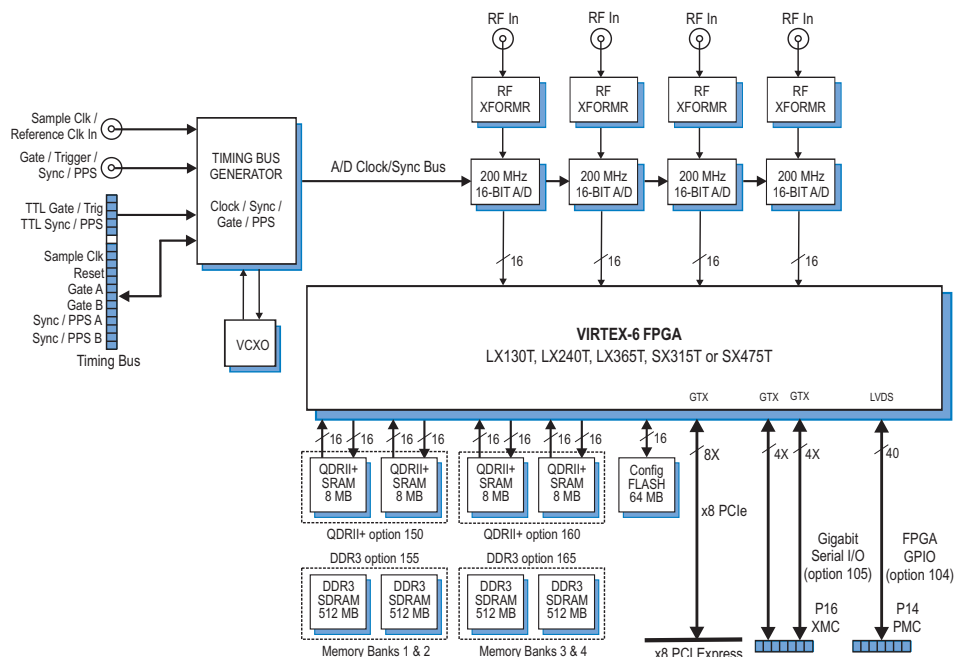
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤



► A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

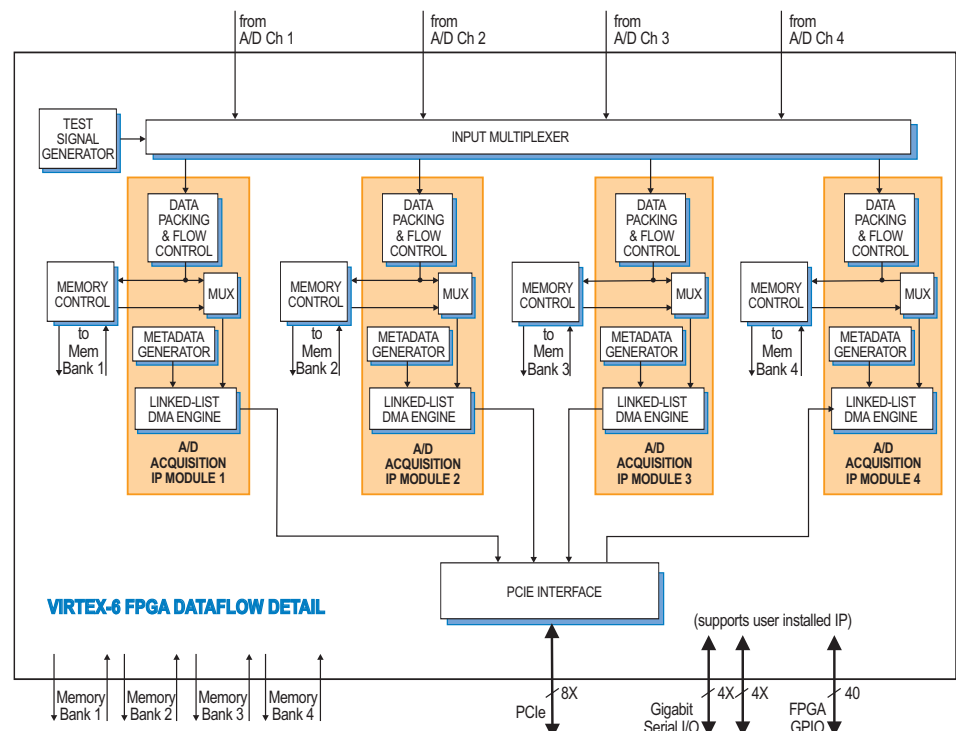
The Model 78660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board. ►

A/D Acquisition IP Modules

The 71660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms,

Function: accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78620 4-Channel 200 MHz A/D with Virtex-6 FPGA - PCIe

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

Rev. 0702

PENTEK

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Tel: 201-818-5900 ♦ Fax: 201-818-5904 ♦ Email: info@pentek.com

www.pentek.com

New!

Model 78661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiband programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78661 is a member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78661 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules

for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

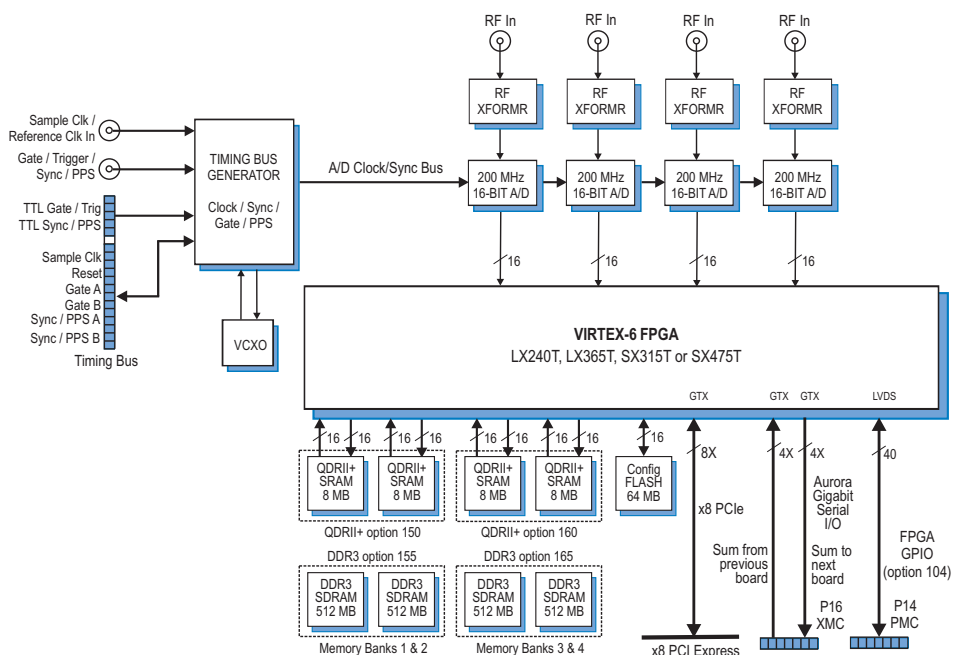
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤



A/D Acquisition IP Modules

The 78661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536

providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Beamformer IP Core

In addition to the DDCs, the 78661 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation

change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

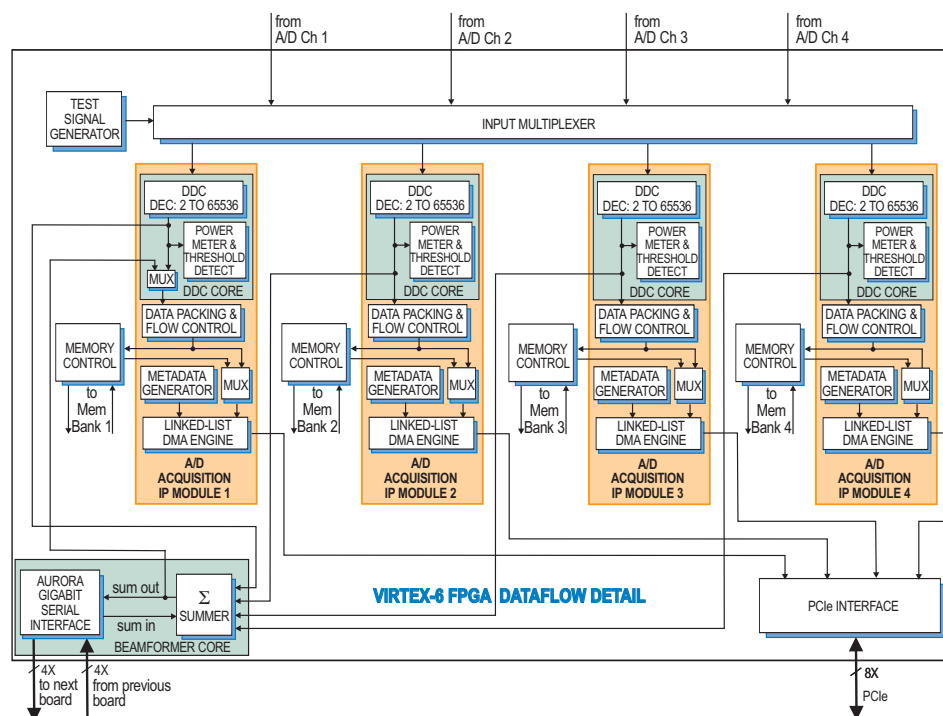
► A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage ►



► controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78661's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Digital Down converters

Quantity: Four channels

Decimation Range: 2 to 65,536 in integer steps

LO Tuning Freq. Resolution: 32 bits, 0 to Fs

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 2 Pi radians

FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms,

Function: 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78621 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

RADAR & SDR I/O - 3U VPX

MODEL	DESCRIPTION
5331	16-Channel Multiband Receiver with A/Ds and FPGA - 3U VPX
5341	Dual Multiband Transceiver with FPGA - 3U VPX
5341-420	Transceiver with Dual Wideband DDC and Interpolation Filter - 3U VPX
5341-430	Transceiver with 256-Channel Narrowband DDC - 3U VPX
5342	Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX
5342-428	Transceiver with Four Multiband DDCs and Interpolation Filter - 3U VPX
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX
5351	256-Channel DDC with four 200 MHz, 16-bit A/Ds - 3U VPX
5352	32-Channel DDC with four 200 MHz, 16-bit A/Ds - 3U VPX
5353	4/2-Channel DDC, four 200 MHz 16-bit A/Ds, Beamformer - 3U VPX
5356	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX
5358	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX
5308	Front Panel x8 PCI Express Adapter - 3U VPX
Cobalt 53620	3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX
Cobalt 53621	3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, 3U VPX
Cobalt 53630	1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX
Cobalt 53650	Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX
Cobalt 53660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX
Cobalt 53661	4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX
	Customer Information

[RADAR & SDR I/O - PMC/XMC](#)

[RADAR & SDR I/O - CompactPCI](#)

[RADAR & SDR I/O - PCI](#)

[RADAR & SDR I/O - x16 PCI Express](#)

[RADAR & SDR I/O - x8 PCI Express](#)

[Click Here for the PRODUCT SELECTOR](#)

Last updated: November 2010



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 80 or 105 MHz, 14-bit A/D converters
- 16 channels of multiband digital downconverters
- 5 kHz to 10 MHz output bandwidth for $f_s = 100$ MHz
- 250 MHz input bandwidth
- Ideal for IF sampling
- User-configurable Xilinx Virtex-II FPGA
- Custom FPGA I/O through the VPX P-2
- Bypass path allows direct capture of A/D data
- LVDS clock/sync bus for multiboard synchronization
- Compatible with several VITA standards including:
VITA-46 (VPX Baseline Standard)
VITA-48 (VPX REDI)
VITA-65 (OpenVPX™ System Specification)

General Information

Model 5331 is a general-purpose 16-channel multiband digital receiver 3U VPX board. It includes both a Virtex-II FPGA and two 14-bit A/Ds for signal processing. The 5331 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane.

Front End

The Model 5331 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors.

The two inputs are transformer coupled and digitized by AD6645 14-bit A/D converters. The AD6645 operates at a maximum sampling rate of 80 MHz in the standard unit and up to 105 MHz for option -100.

The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, or from an external sample clock supplied through a front panel SMA connector or the front panel sync bus.

Digital Downconverters

The 5331 includes four TI/Graychip GC4016 quad multiband digital downconverter chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable

channels capable of center frequency tuning from DC to $f_s/2$, where f_s is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from the two A/D converters. A crossbar switch in each GC4016 allows all 16 channels on the board to select either of the two A/D inputs for flexible switching.

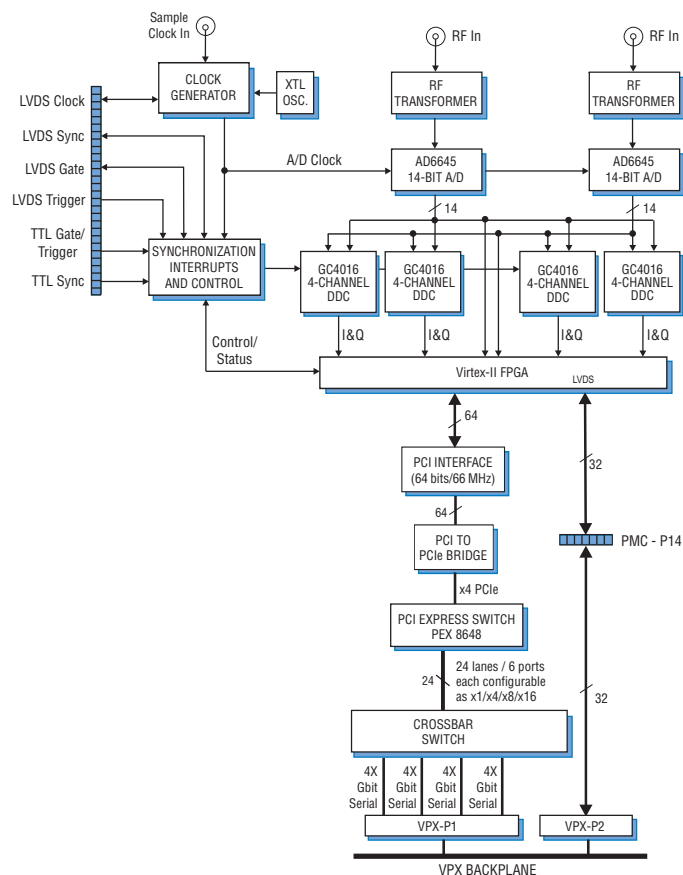
Output Bandwidth

With a 100 MHz sample clock, the useable output bandwidth of each of the downconverter channels is 2.5 MHz. However, since the Model 5331 delivers parallel digital outputs from the GC4016 into the FPGA, users can take advantage of the GC4016 channel combining mode to join two or four channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.

Since both A/D converters connect directly to the FPGAs, signals with even wider bandwidths can be accommodated.

FPGA

The downconverter outputs are delivered to a Xilinx Virtex-II XC2V1000 FPGA (XC2V3000 with option -300) which is factory configured to perform various modes of data packing, formatting and channel selection. ➤



Fabric-Transparent Crossbar Switch

The 5331 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

► Dual-port memories in the FPGA provide efficient transfers by buffering receiver and A/D data. The A/D outputs are also connected directly to the FPGA so that wideband A/D data can be delivered directly to the baseboard bypassing the downconverters. An A/D decimation mode allows one of every N samples to be written into the FPGA memory, where N is any integer between 1 and 4096. This overcomes the lower frequency limit on the A/D sample clock.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the FPGA. Option -5xx adds four full duplex 4X gigabit serial paths to VPX-P1 connector.

Synchronization

The front panel clock and sync bus allow one 5331 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple boards.

Up to eight slave 5331's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. In addition to the LVDS timing bus, the Model 5331 can receive front panel TTL input signals for gate or trigger functions.

Interrupt Sources

The Model 5331 has several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload output codes, transitions on the gate signals, clock loss, buffer swapping, or a programmable over-temperature condition or faulty power supply voltage. The ADM1024 Voltage/Temperature Monitor provides constant monitoring of critical voltages and temperatures and generates an interrupt if values exceed threshold limits which are user programmable over the VPX backplane.

PCI Express Switch

Model 5331 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMA connectors

Transformer Type: Mini-Circuits ADT4-6T

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 270 MHz

A/D Converters, Standard

Type: Analog Devices AD6645-80

Sampling Rate: 30 MHz to 80 MHz

Internal Clock: 80 MHz crystal osc.

External Clock: 30 to 80 MHz

Resolution: 14 bits

A/D Converters, Option -100

Type: Analog Devices AD6645-105

Sampling Rate: 30 MHz to 105 MHz

Internal Clock: 100 MHz crystal osc.

External Clock: 30 to 105 MHz

Resolution: 14 bits

Clock Source: Onboard crystal oscillator, front panel ext clock, or LVDS clock

External Clock

Type: Front panel female SMA connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms impedance

Sync/Gate Bus

Type: 26-pin connector, with one clock, one sync, and two gate input/output LVDS signals; two trigger LVDS inputs; and one sync and one gate input TTL signals

Digital Downconverters

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D outputs are connected to all GC4016's

Output: Parallel complex data

Bypass Mode: Data from the A/D converters can be written directly into the FPGAs at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096

Field Programmable Gate Array

Type: Xilinx Virtex-II XC2V1000 standard

Option -300: Virtex-II XC2V3000

Option -104: Installs the P4 connector with 37 lines to the XC2V1000 or 64 lines to the XC2V3000 FPGA

Dual Port RAM Data Buffers

Size: 4k x 32 DPRAM expandable to 8k x 32 with option -300 FPGA

PCI to PCIe Interface

Type: PLX Technology PCI 9656

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)

Gigabit Serial I/O:

VPX-P1: Four 4X ports to Crossbar Switch
PCI Express: Six ports to Crossbar Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5331	16-Channel Multiband Receiver with A/Ds and FPGA - PMC
Options:	
-100	105 MHz A/D with 100 MHz crystal oscillator
-104	FPGA I/O to VPX-P2
-300	XC2V3000 FPGA
-5xx	Gigabit Serial I/O to VPX-P1 - four full-duplex 4X paths

New!

Model 5341

Dual Multiband Transceiver with FPGA - 3U VPX



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 125 MHz 14-bit A/Ds
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O
- Compatible with several VITA standards including:
VITA-46 (VPX Baseline Standard)
VITA-48 (VPX REDI)
VITA-65 (OpenVPX™ System Specification)

General Information

Model 5341 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters, and is capable of bandwidths to 50 MHz and above.

The 5341 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

The 5341 features a TI/Graychip GC4016 quad digital downconverter, accepting either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/Ds, FPGA signal

processing engine, SDRAM delay memory and data sources on the VPX backplane.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

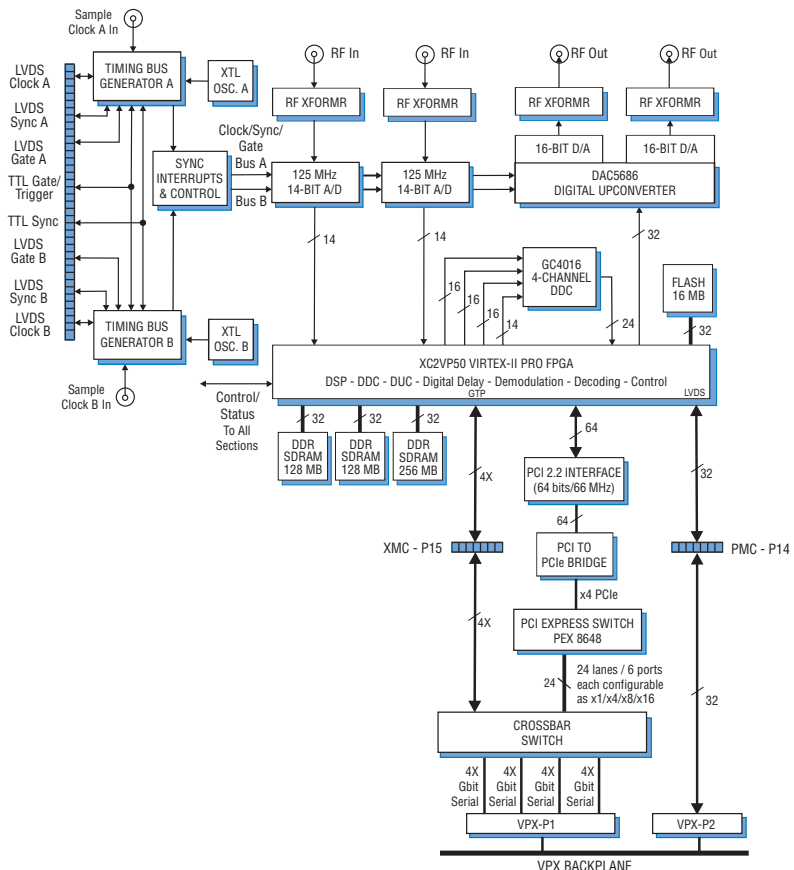
A TI DAC5686 digital upconverter and dual D/A is attached to the FPGA, accepting baseband real or complex data streams with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGAs

A Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with ➤



Fabric-Transparent Crossbar Switch

The 5341 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

PCI Express Switch

Model 5341 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Ordering Information

Model	Description
5341	Dual Multiband Transceiver with FPGA - 3U VPX
Options:	
-002	Full-scale output: -2 dBm into 50 ohms; 3 dB passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O to VPX-P2
-125	125 MHz Bus A and 100 MHz Bus B internal oscillators
-420	Dual wideband DDC and digital interpolation filter cores, factory-installed in FPGA
-430	256-channel narrowband DDC core, factory-installed in FPGA
-5xx	Gigabit Serial I/O to VPX-P1 - four full-duplex 4X paths

► data and programming interfaces to each of the on-board resources including the A/D converters, digital downconverter, digital upconverter and D/A converters. Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the FPGA. Option -5xx adds four full duplex 4X gigabit serial paths to VPX-P1 connector.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the corresponding input and output signals.

Each timing bus includes a clock, sync, and gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the A/Ds, downconverter, upconverter and D/As. Two external reference clocks or two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 5341 boards can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available to the FPGA (to 1 GB max.). Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB
Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255
Sampling Rate: 1 MHz to 125 MHz
Internal Clock: Crystal osc. (2 per A/D)
External Clock: 1 to 125 MHz
Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
Option -002: -2 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz
Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clocks

Type: Female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohm

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro
Option -050: XC2VP50
Option -104: 64 lines (32 pairs)

Memory

DDR SDRAM: 512 MB in three banks
FLASH: One bank of 16 MB

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz
DMA: 9-channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

FPGA: One 4X port to Crossbar Switch
VPX-P1: Four 4X ports to Crossbar Switch
PCI Express: Six ports to Crossbar Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental (Commercial version)

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Model 5341-420 Installed Core

GateFlow Transceiver with Dual Wideband DDCs and Interpolation Filter - 3U VPX



ReadyFlow
Board Support Package

Features

- Complete software radio interface solution
- 3U VPX form factor
- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz
- LVDS clock/sync bus for multiboard synchronization

General Information

Model 5341-420 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters with built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch bridges numerous interfaces and components on the board with no latency.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital down-converter.

The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGA and to other board resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, this board includes Pentek's GateFlow installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 down-converter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and

formatter deliver output data in either real or complex representation. An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

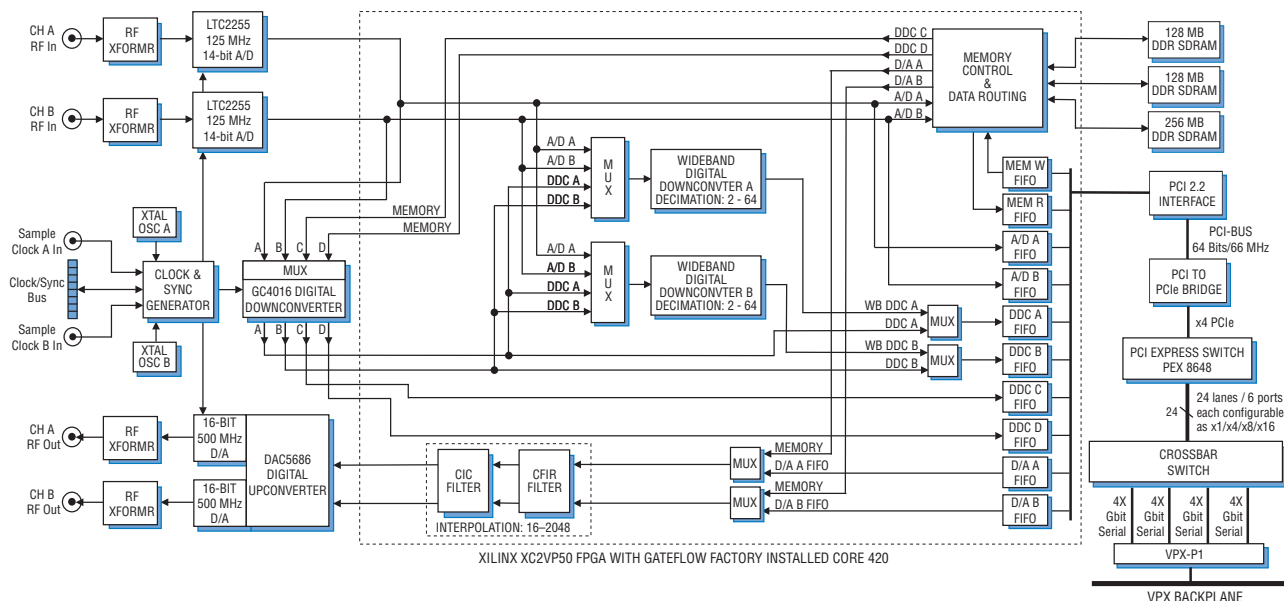
Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of the Model 5341 are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤



Fabric-Transparent Crossbar Switch

The 5341-420 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 5341-420's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Switch

Model 5341-420 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

Ordering Information

Model	Description
5341-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - 3U VPX

Contact Pentek for available options

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

FLASH: One bank of 16 MB

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Gigabit Serial I/O

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Model 5341-430 Installed Core

GateFlow Transceiver, 256-Channel Narrowband DDC - 3U VPX



Features

- Complete software radio interface solution
- 3U VPX form factor
- GateFlow Core 430 with 256 channels of narrowband digital downconverters factory-installed
- 256 programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256
- LVDS clock/sync bus for multiboard synchronization

General Information

Model 5341-420 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters with built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch bridges numerous interfaces and components on the board with no latency.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital down-converter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGA and to other board resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 5341-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter

coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

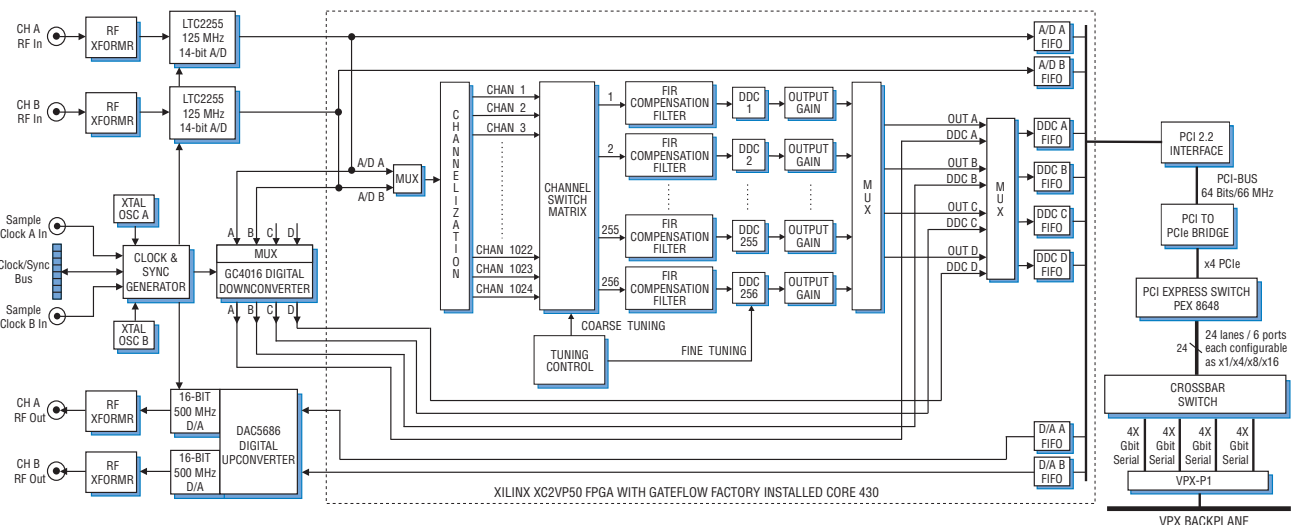
Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Performance Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit Complex
Tuning Resolution	Clock Freq / 2 ³²
Decimation	1024 – 9984 in steps of 256
Passband Ripple	<0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	>75 dB
NCO SFDR	>110 dB

Flexible Architecture

Core 430 DDC comes factory-installed in this Model. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any interger value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤



Fabric-Transparent Crossbar Switch

The 5341-430 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

► Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 5341-430's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Switch

Model 5341-430 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: Crystal oscillator A or B

External Clock: 1 to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016

Decimation: 32 to 16,384; with channel combining mode: 8 or 16

Data Source: A/D, FPGA, or PCI interface

Control Source: FPGA or PCI interface

Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro XC2VP50

Memory

DDR SDRAM: 512 MB in three banks

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Gigabit Serial I/O

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5341-430	GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 3U VPX

Contact Pentek for available options

New!

Model 5342

Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 125 MHz 14-bit A/Ds
- One digital upconverter
- One 500 MHz 16-bit D/A
- Two Xilinx Virtex-4 FPGAs
- Up to 768 MB of DDR2 SDRAM
- LVDS clock/sync bus for multiboard synchronization
- Optional factory-installed IP Cores available
- Up to 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
VITA-46 (VPX Baseline Standard)
VITA-48 (VPX REDI)
VITA-65 (OpenVPX™ System Specification)

General Information

Model 5342 is a multichannel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds with one upconverter and D/A converter.

The 5342 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into a Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

The 5342 features a TI DAC5686 digital upconverter (DUC) and D/A. It accepts a base-band real or complex data stream from its FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, the DAC5686 interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160

MHz. It delivers real or quadrature (I+Q) analog outputs up to 320 MHz to the 16-bit D/A converter. If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

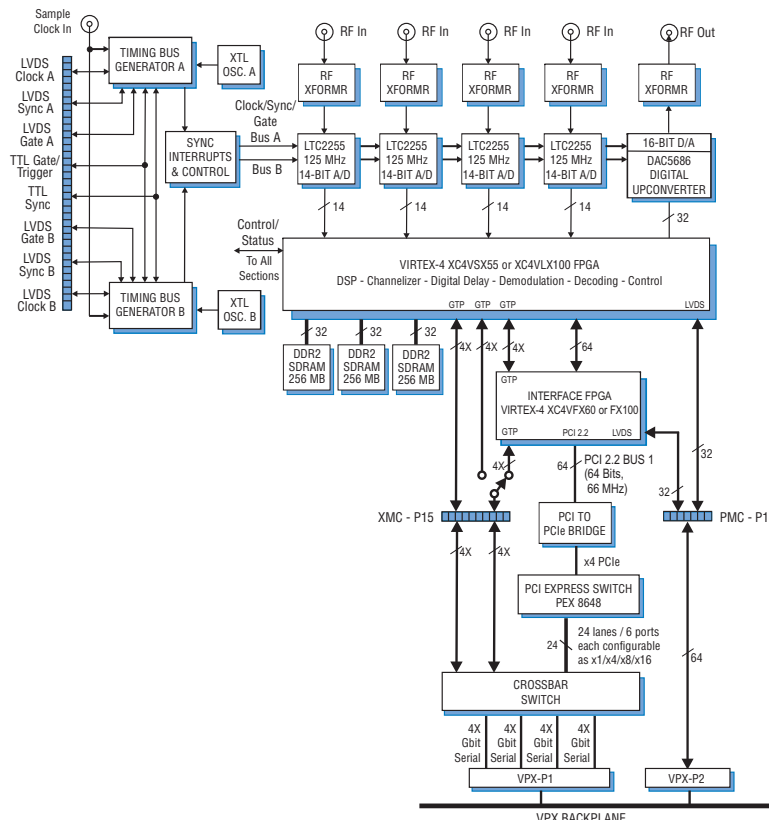
Virtex-4 FPGAs

The 5342 architecture includes two Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can include their own custom IP, and integrate it with factory-shipped functions using a Pentek GateFlow FPGA Design Kit.

The Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for implementing functions such as demodulation/modulation, digital delay and channelization. For applications requiring more FPGA logic cells, the Model 5342 can be optionally configured with XC4VLX100 for up to 221,184 logic cells.

A Virtex-4 XC4VFX60 Interface FPGA provides board interfaces including PCI ➤



Fabric-Transparent Crossbar Switch

The 5342 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

PCI Express Switch

Model 5342 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Ordering Information

Model Description

5342 Multichannel Transceiver with four A/Ds, one D/A and Virtex-4 FPGAs - 3U VPX

Options:

-100 XC4VFX100 replaces XC4VFX60
 -104 FPGA I/O to VPX-P2
 -110 XC4VLX100 replaces XC4VSX55
 -428 Four multiband DDCs and interpolation filter, factory-installed core in the processing FPGA
 -5xx Gigabit Serial I/O to VPX-P1- four full-duplex 4X paths

and serial I/O.

The interface FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. The Model 5342 can be optionally configured with XC4VFX100 in place of each FX60.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the A/Ds, upconverter and D/A. Internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, each LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 5342s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to the SX55 or LX100 FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal osc.

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms (other options available)

3 dB Passband: 60 kHz to 300 MHz (other options available)

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-4 XC4VSX55 & Xilinx Virtex-4 XC4VFX60

Option -100: XC4VFX100 replaces XC4VFX60

Option -110: XC4VLX100 replaces XC4VSX55

Custom I/O

Option -104: Adds GPIO connector with 32 lines to the XC4VFX60/100 FPGA

Memory

DDR2 SDRAM: 768 MB in three banks to SX55/LX100 FPGA

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

Processing FPGA: Two 4X ports to Fabric-Transparent Switch; one can be alternately routed to interface FPGA

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Model 5342-428 Installed Core

GateFlow Transceiver with Four Multiband DDCs and Interpolation Filter - 3U VPX



Features

- Complete software radio interface solution
- 3U VPX form factor
- GateFlow IP Core 428, with four high-performance multiband DDCs and one Interpolation Filter, factory-installed
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4
- LVDS clock/sync bus for multiboard synchronization

General Information

Model 5342-428 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters with built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch bridges numerous interfaces and components on the board with no latency.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other board resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating

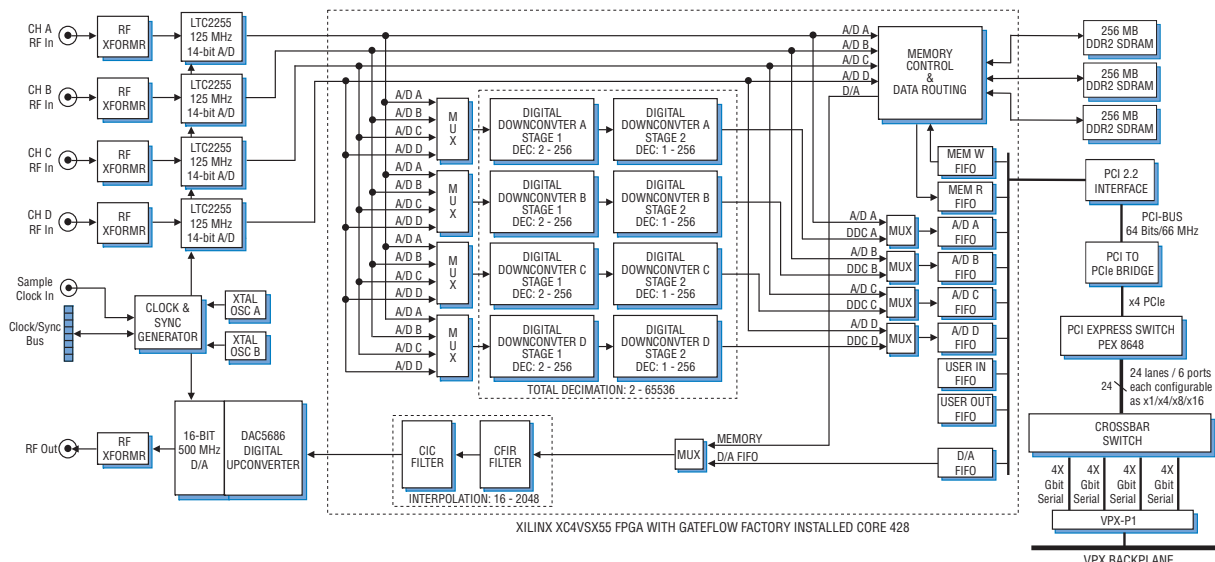
FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 5342-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ➤



Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 5342-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

Fabric-Transparent Crossbar Switch

The 5342-428 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

PCI Express Switch

Model 5342-428 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255

Sampling Rate: 1 MHz to 125 MHz

Internal Clock: 125 MHz crystal oscillator

External Clock: 1 to 125 MHz

Resolution: 14 bits

A/D Data Reduction Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Arrays

Type: Xilinx Virtex-4 XC4V5X55 and

Xilinx Virtex-4 XC4VFX60

Memory

DDR2 SDRAM: 768 MB in three banks of 256 MB each

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz

DMA: 9 channel demand-mode and chaining controller

Gigabit Serial I/O

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental (Commercial version)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5342-428	GateFlow Transceiver with four Multiband DDCs and one Interpolation Filter factory-installed - 3U VPX

Contact Pentek for available options

New!

Model 5350

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX



Model 5350 commercial (left) and conduction-cooled version



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- Up to 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
VITA-46 (VPX Baseline Standard)
VITA-48 (VPX REDI)
VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 5350 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds. These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 5350 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other board resources.

Virtex-5 FPGAs

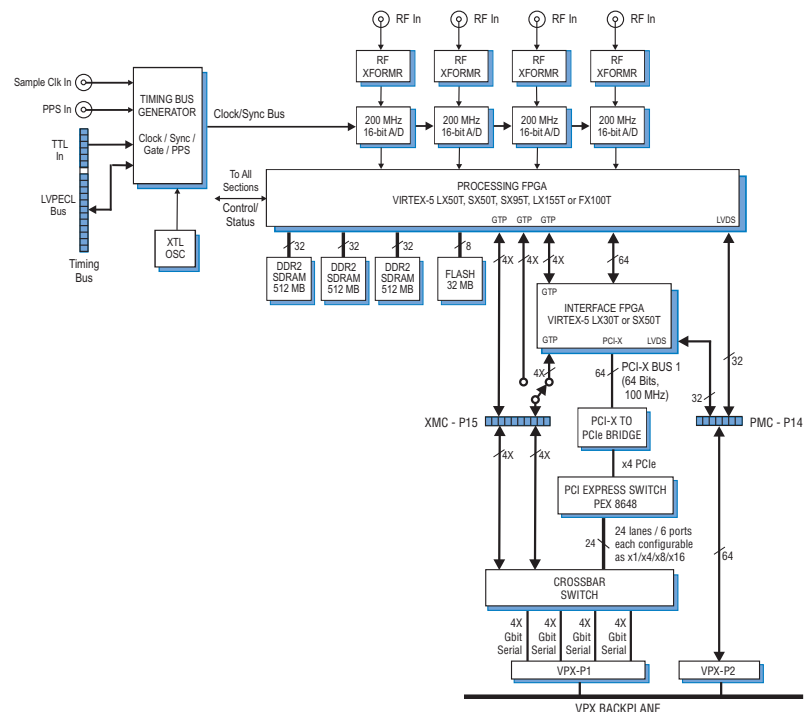
The Model 5350 architecture includes two Virtex-5 FPGAs. All data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP.

There are two FPGA types on the 5350: processing and interface. The processing FPGA serves as a control and status engine with data and programming interfaces to each of the onboard resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 5350 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express, preserving the processing FPGA resources for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O. ➤



Clocking and Synchronization

The Model 5350 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 5350s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Two of the banks support built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. These banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of all three banks to support various applications.

Fabric-Transparent Crossbar Switch

The 5350 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

PCI Express Switch

Model 5350 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX50T standard; XC5VLX50T, XC5VSX95T, XC5VLX155T or XC5VFX100T, optional

Interface FPGA: Xilinx Virtex-5 XC5VLX30T std.; XC5VSX50T optional

Custom I/O

Option -104: Provides GPIO to VPX-P2 with 16 LVDS pairs to processing FPGA (SX95T, LX155T or FX100T only) and 16 pairs to interface FPGA

Memory

DDR2 SDRAM: to 1.5 GB in three banks

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

Processing FPGA: Two 4X ports to Fabric-Transparent Switch; one can be alternately routed to interface FPGA

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:

Forced-Air Cooled: 0° to 50° C std;
-20° to 65° C (Level L2)

Conduction-Cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX
Options:	
-104	FPGA I/O to VPX-P2
-5xx	Gigabit Serial I/O to VPX-P1- four full duplex 4X paths
-703	Level L3 Conduction-Cooled Version

Contact Pentek for additional available options.

New!

Model 5351

256-Channel DDC with Four 200 MHz, 16-bit A/Ds - 3U VPX



ReadyFlow
Board Support Package

Features

- 256 DDC channels
- Four 200 MHz 16-bit A/Ds
- Independent tuning for each channel and decimation for each bank
- DDC decimation from 128 to 1024 in steps of 64
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Each bank independently selects one of four A/Ds
- LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor with ruggedized and conduction-cooled versions available

General Information

Model 5351 is a high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds. The A/D converters are supported by a high-performance 256-channel installed DDC (digital downconverter) IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 5351 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer-coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 5351 SX95T FPGA employs an advanced FPGA-based digital down-converter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the attached four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

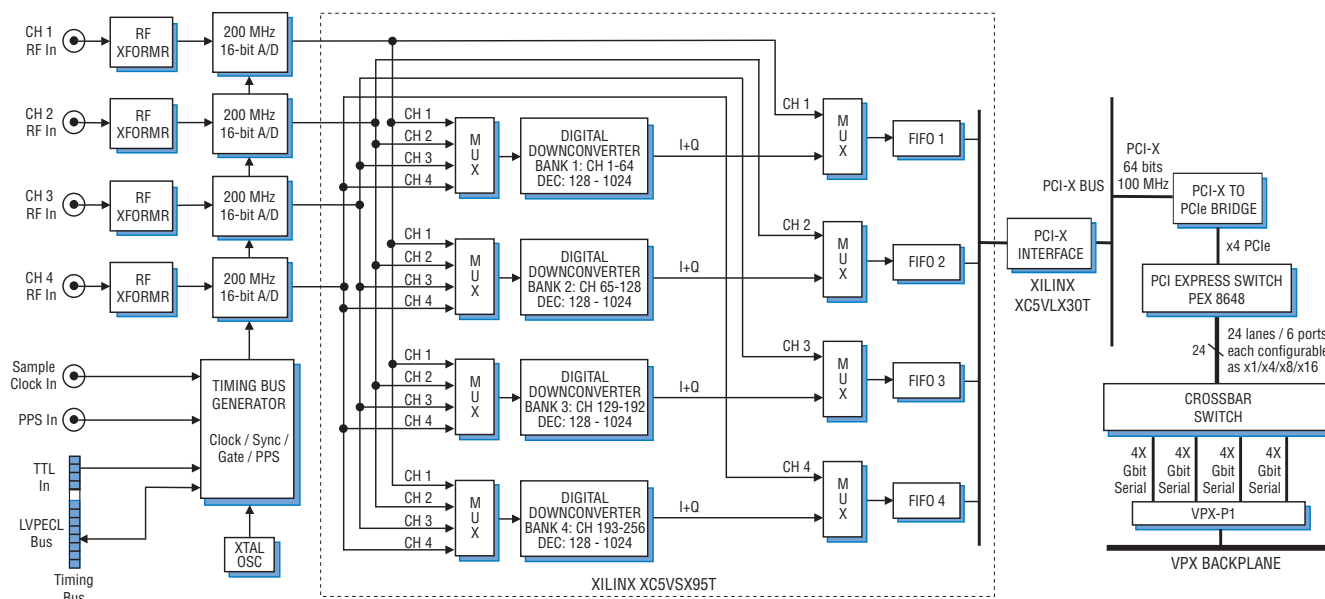
All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Output Multiplexers and FIFOs

Four output MUXs in the SX95T FPGA can be independently switched to deliver either A/D or DDC data into each output FIFO. This allows users to view either ➤



wideband A/D data or narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 5351 architecture includes a flexible timing and synchronization circuit for the bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connectors allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 5351's can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Fabric-Transparent Crossbar Switch

The 5351 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

PCI Express Switch

Model 5351 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX95T dedicated to digital downconverters and output

Interface FPGA: Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:

Forced-Air Cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-Cooled: -40° to 70°C (Level L3)

Storage Temperature:

Forced-Air Cooled: -20° to 90° C std;

-40° to 100° C (Level L1, L2)

Conduction-Cooled: -50° to 100°C (L3)

Relative Humidity: 0 to 95%, non-cond.; 0 to 100% with conformal coating

Size: 3.937 in. x 6.717 in. (100 mm x 170.6mm)

Ordering Information

Model	Description
5351	256-Channel DDC with four 200 MHz, 16-bit A/D - 3U VPX
Options:	
-703	Level L3 Conduction-Cooled Version
-731	Two-slot heat sink

Contact Pentek for additional available options.

New!

Model 5352

32-Channel DDC with Four 200 MHz, 16-bit A/Ds - 3U VPX



ReadyFlow
Board Support Package

Features

- 32 channels of DDC in banks of 8 channels
- Independent 32-bit DDC tuning for all channels
- DDC decimation from 16 to 8192 in steps of 8
- Bandwidths from 20 kHz to 10 MHz
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor with ruggedized and conduction-cooled versions available

General Information

Model 5352 is a high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds. The A/Ds are supported by a high-performance 32-channel installed DDC (digital downconverter) IP Core, and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 5352 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 5352 SX95T FPGA employs an advanced FPGA-based digital down-converter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four attached A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDCs has an independent 32-bit tuning frequency setting ranging from DC to f_s (f_s is the A/D sample rate).

Decimation and Filtering

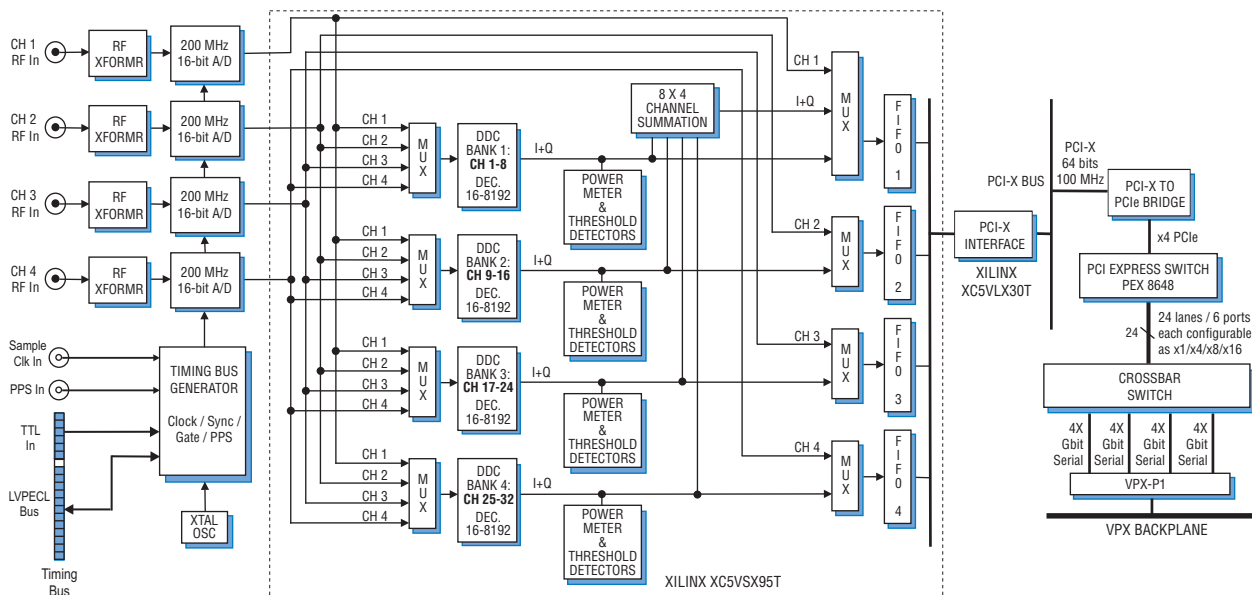
All of the eight channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have a unique decimation setting supporting up to four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. Rejection of adjacent-band components within the 80% bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters and Threshold Detectors

The 5352 features 32 power meters that continuously measure the individual average power output of each DDC channel. The time constant of the averaging interval is programmable up to 16 kilosamples. In addition, threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold. ➤



Output Multiplexers and FIFOs

Four output MUXs in the SX95T FPGA can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application. Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 5352 architecture includes a flexible timing and synchronization circuit for the group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 5352's can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

Fabric-Transparent Crossbar Switch

The 5352 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

PCI Express Switch

Model 5352 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX95T dedicated to digital downconverters and output

Interface FPGA: Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:

Forced-Air Cooled: 0° to 50° C std;
-20° to 65° C (Level L2)

Conduction-Cooled: -40° to 70° C (Level L3)

Storage Temperature:

Forced-Air Cooled: -20° to 90° C std;
-40° to 100° C (Level L1, L2)

Conduction-Cooled: -50° to 100° C (L3)

Relative Humidity: 0 to 95%, non-cond.;
0 to 100% with conformal coating

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5352	32-Channel DDC with four 200 MHz, 16-bit A/Ds - 3U VPX

Options:

-703	Level L3 Conduction-Cooled Version
-731	Two-slot heat sink

Contact Pentek for additional available options.

New!

Model 5353

4/2-Ch. DDC, four 200 MHz 16-bit A/Ds, Beamformer - 3U VPX



ReadyFlow
Board Support Package

Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- Four 200 MHz, 16-bit A/Ds
- 2 or 4 Channels of DDC
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor with ruggedized and conduction-cooled versions available

General Information

Model 5353 is a high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel installed DDC (digital downconverter) and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

The 5353 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 5353 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency.

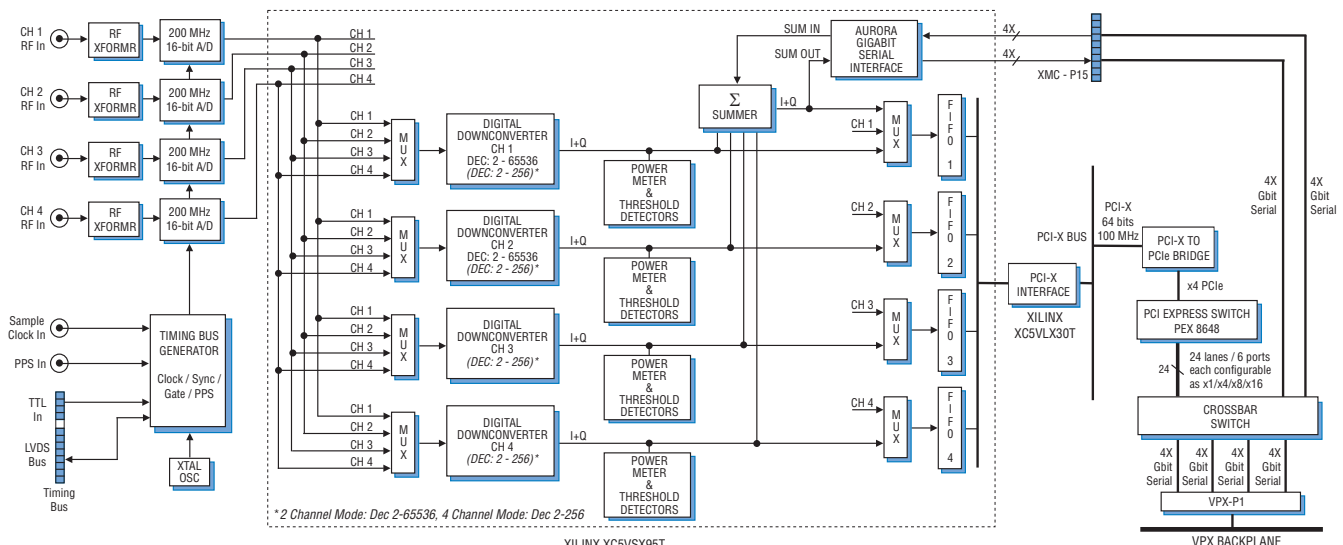
Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N .

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications. ➤



VPX Interface

For large systems, multiple 5353's can be chained together via a built-in Xilinx Aurora interface through the VPX-P1 connector.

This link creates a board-to-board summation expansion chain for creating larger multi-channel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

Beamformer

In addition to the A/Ds and DDCs, the 5353 includes essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCIe interface out to the VPX backplane.

For larger systems, multiple 5353's can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates a x4 sum output stream to the next board through the VPX-P1 connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input and output rates to support different DDC decimation settings between the banks and efficient block transfers to the PCI-X bus.

Clocking and Synchronization

The Model 5353 architecture includes a flexible timing and synchronization circuit

for the group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

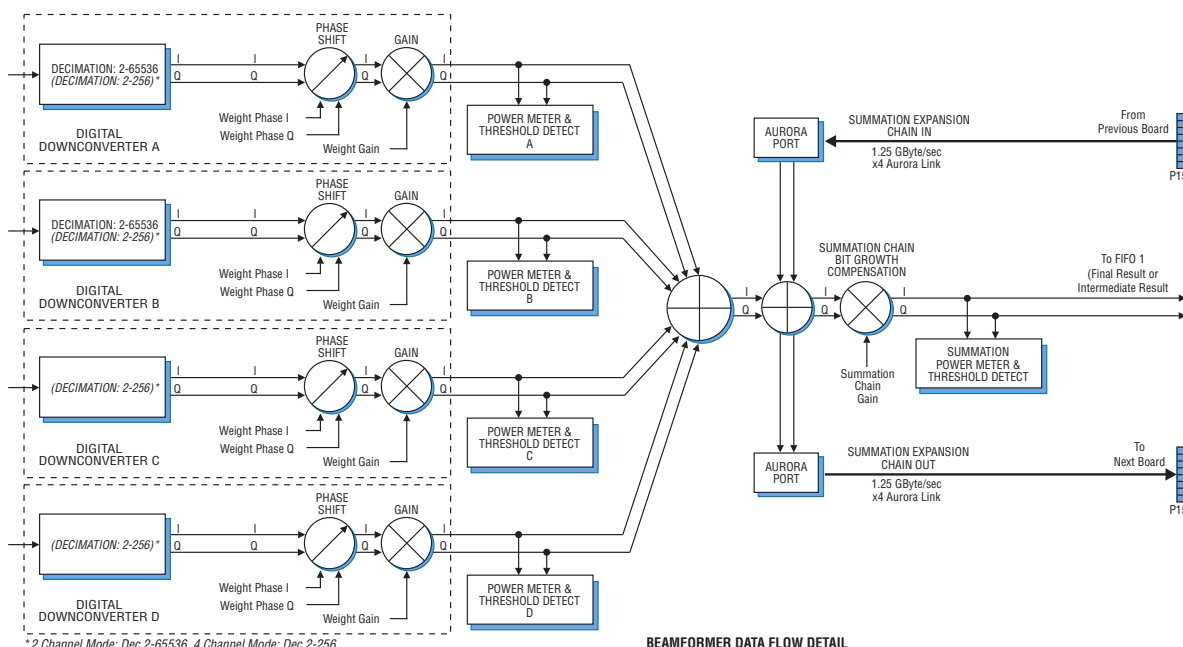
The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 5353's can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

Fabric-Transparent Crossbar Switch

The 5353 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).



PCI Express Switch

Model 5353 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillator, external reference or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS, input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Digital Downconverter

Type: IP core for Xilinx Virtex-5

Qty of DDC Channels: 2 or 4

Center Frequency Tuning: 4 tuning words, one for each DDC channel

Center Frequency Tuning Range: DC to f_s with 32 bit resolution

NCO SFDR: -120 dBFS

Channel Phase Offset Adjustment:

32-bit resolution

Channel Gain Adjustment: 32-bit resolution

Input Selection for DDC Banks: Any channel can select any of the four A/Ds

Decimation Range (N):

2-Channel Mode: 2 to 65536

4-Channel Mode: 2 to 256

FIR Filter: Default passband $0.8 \cdot f_s / N$ with 0.2 dB passband ripple and 100 dB adjacent channel rejection

FIR Filter Coefficients: 18 bits, user-programmable (default values provided)

Qty FIR Filter Taps: $28 \cdot N / 8$

Output Format: 24 bits I + 24 bits Q

Output Spectrum Modes: Normal or frequency-reversed

Output Spectrum Offset: No offset or offset by one-half the output bandwidth

Beamformer

Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain

Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion: 32-bit

Output Multiplexer and FIFO

Qty Output FIFOs: Four

FIFO Source Selection: Independent multiplexer selects DDC output or A/D

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

Processing FPGA: Two 4X ports to Aurora Gigabit Serial Interface

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:

Forced-Air Cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-Cooled: -40° to 70° C (Level L3)

Storage Temperature:

Forced-Air Cooled: -20° to 90° C std;

-40° to 100° C (Level L1, L2)

Conduction-Cooled: -50° to 100° C (L3)

Relative Humidity: 0 to 95%, non-cond.; 0 to 100% with conformal coating

Size: 3.937 in. x 6.717 in. (100 mm x 170.6mm)

Ordering Information

Model	Description
5353	4/2-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - 3U VPX
Options:	
-5xx	Gigabit Serial I/O to VPX-P1- four full-duplex 4X paths
-703	Level L3 Conduction-Cooled Version
-730	Two-Slot Heat Sink

Contact Pentek for additional available options.

New!

Model 5356

Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 400 MHz 14-bit A/Ds
- One DUC (Digital Upconverter)
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
 - VITA-46 (VPX Baseline Standard)
 - VITA-48 (VPX REDI)
 - VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 5356 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communication system. It includes two 400 MHz A/Ds, 800 MHz D/A and Virtex-5 FPGAs.

The 5356 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TIADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the processing FPGA for signal processing, capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter.

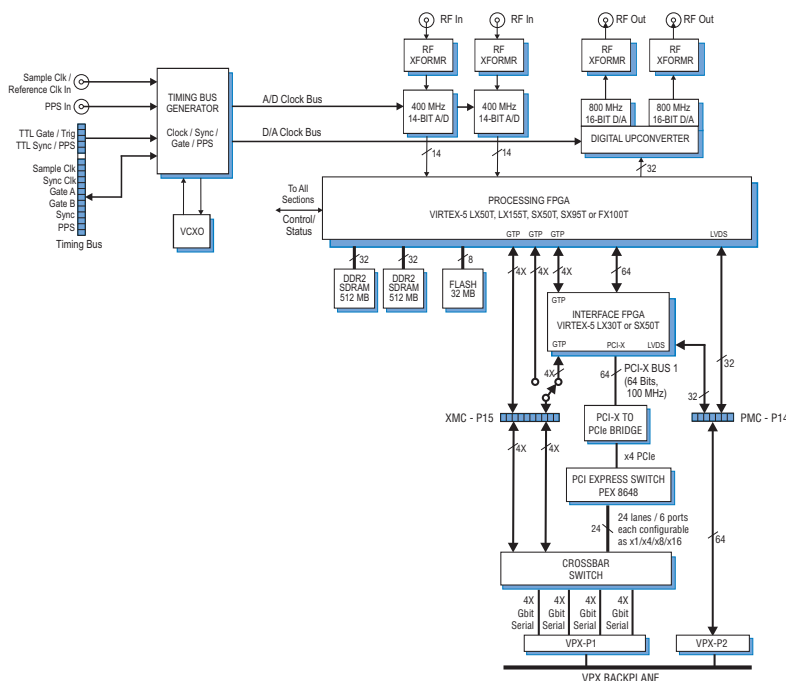
Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC provides interpolation factors of 2x, 4x and 8x.

Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between ➤



Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGAs. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Fabric-Transparent Crossbar Switch

The 5356 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

PCI Express Switch

Model 5356 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Ordering Information

Model	Description
5356	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX
Options:	
-104	FPGA I/O to VPX-P2
-5xx	Gigabit Serial I/O to VPX-P1- four full-duplex 4X paths
-703	Level L3 Conduction-Cooled Version

Contact Pentek for additional available options.

reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the processing FPGA, and 16 more to the interface FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 5356's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5474

Sampling Rate: 20 MHz to 400 MHz

Resolution: 14 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 20 to 400 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Option -104: Provides GPIO to VPX-P2 with 16 LVDS pairs to processing FPGA (SX95T, LX155T or FX100T only) and 16 pairs to interface FPGA

Memory

DDR2 SDRAM: Up to 1.0 GB in two banks to processing FPGA

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

Processing FPGA: Two 4X ports to Fabric-Transparent Switch; one can be alternately routed to interface FPGA

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:

Forced-Air Cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-Cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Model 5358

Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 500 MHz 12-bit A/Ds
- One DUC (Digital Upconverter)
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
VITA-46 (VPX Baseline Standard)
VITA-48 (VPX REDI)
VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 5358 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communication system. It includes two 500 MHz A/Ds, 800 MHz D/A and Virtex-5 FPGAs.

The 5358 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TIADS5463 12-bit 500 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the processing FPGA for signal processing, capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter.

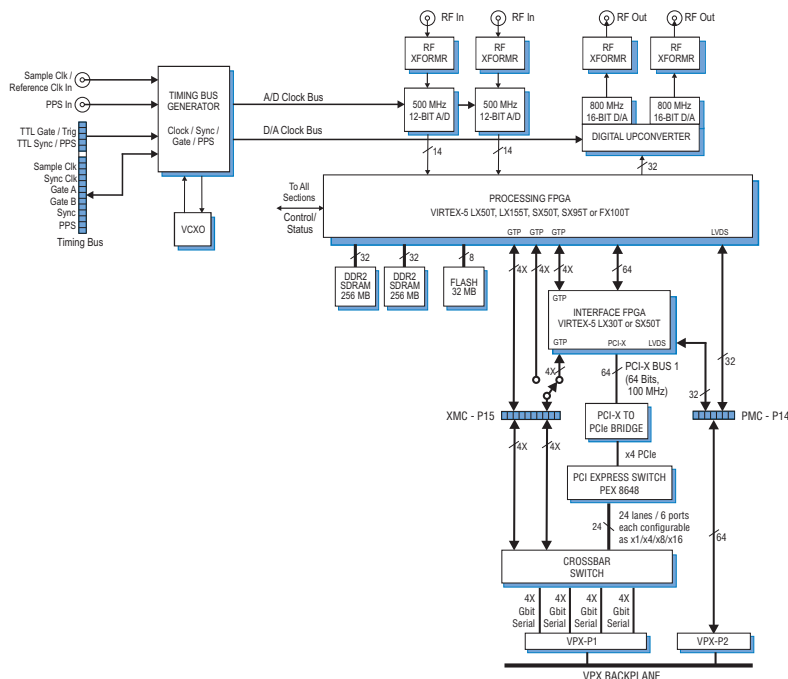
Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC provides interpolation factors of 2x, 4x and 8x.

Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between ➤



Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGAs. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Fabric-Transparent Crossbar Switch

The 5358 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

PCI Express Switch

Model 5358 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Ordering Information

Model	Description
5358	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX
Options:	
-104	FPGA I/O to VPX-P2
-140	1 GB DDR2 SDRAM
-5xx	Gigabit Serial I/O to VPX-P1- four full-duplex 4X paths
-703	Level L3 Conduction-Cooled Version

Contact Pentek for additional available options.

► reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the processing FPGA, and 16 more to the interface FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 5358's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: TI ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

D/A Converters

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms, accepts 20 to 500 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays

Processing FPGA: Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Option -104: Provides GPIO to VPX-P2 with 16 LVDS pairs to processing FPGA (SX95T, LX155T or FX100T only) and 16 pairs to interface FPGA

Memory

DDR2 SDRAM: Up to 1.0 GB in two banks to processing FPGA

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

Processing FPGA: Two 4X ports to Fabric-Transparent Switch; one can be alternately routed to interface FPGA

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:

Forced-Air Cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-Cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

New!

Model 5308

Front Panel x8 PCI Express Adapter - 3U VPX



Features

- Front Panel x8 PCI Express connection to host PC
- 3U VPX form factor provides a compact, rugged platform
- Cascade mode provides connection to an additional VPX system
- Compatible with several VITA standards including:
VITA-46 (VPX Baseline Standard)
VITA-48 (VPX REDI)
VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Ordering Information

Model	Description
5308	Front Panel x8 PCI Express Adapter - 3U VPX

Options:

-001	Host Adapter Mode (for connection to external host computer)
-002	Cascade Mode (for connection to additional VPX system)
-703	Level L3 Conduction-Cooled Version

Accessories:

Model	Description
4235	PCI Express x8 Host Card for PC
2180	PCI Express x8 Cable

General Information

Model 5308 is a front panel PCI Express adapter for 3U VPX systems. It provides a convenient interface from a 3U VPX system to an external host computer, to simplify development.

The 5308 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration allows selection of the desired VPX-P1 port.

Front Panel Connection

The 5308 provides a front panel interface to the 3U VPX system for connection to a host computer. It supports x4 or x8 PCIe protocol in compliance with PCI-SIG PCI Express® External Cabling 1.0 Specification. It can also be used to connect to an additional VPX system when ordered with Cascade Mode (option -002).

Model 5308 contains built-in PCI Express ReDriver™ circuitry. This circuitry provides signal conditioning that allows the user to correct for signal loss or data errors due to cable length.

PC Connection

The most common use for Model 5308 is for connection to an external host computer. In order to make this connection, the PC requires a PCIe host adapter which is also compliant to PCI-SIG PCI Express External Cabling 1.0 Specification. Adapters supporting either PCIe x8 Gen. 1 or Gen. 2 are available from Pentek under Model 4235.

Fabric-Transparent Crossbar Switch

Two ports from the front panel PCI Express connector are attached to a Fabric-Transparent Crossbar switch. This switch bridges numerous interfaces on the board using gigabit serial data paths with no latency. This allows the user to select the desired port on VPX-P1.

Data paths can be selected as single (x1) lanes, or groups of four lanes (x4). Programmable signal input equalization and output pre-emphasis settings enable optimization. A USB interface is provided for switch programming, and 4 MB onboard FLASH memory allows storage of up to 16 user configurations. Several useful configurations are pre-installed at the factory.

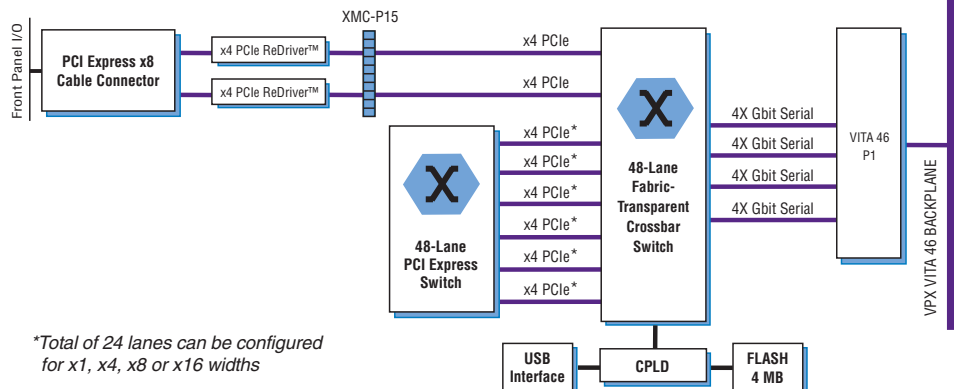
PCI Express Switch

The 5308 includes a multiport PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the fabric-transparent crossbar switch. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Data to or from the panel cable can be selected as x4 or x8 width. Both PCIe Gen. 1 and Gen. 2 are supported.

3U VPX Interface

The 5308 provides full-duplex links to the VPX P1 connector, each capable of peak rates up to 1 gigabyte per sec. Four sets of x4 links support PCI Express.



New!

Model 53620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX



Model 53620 COTS (left)
and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53620 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53620 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board's analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator,

and a PCIe interface complete the factory-installed functions and enable the 53620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

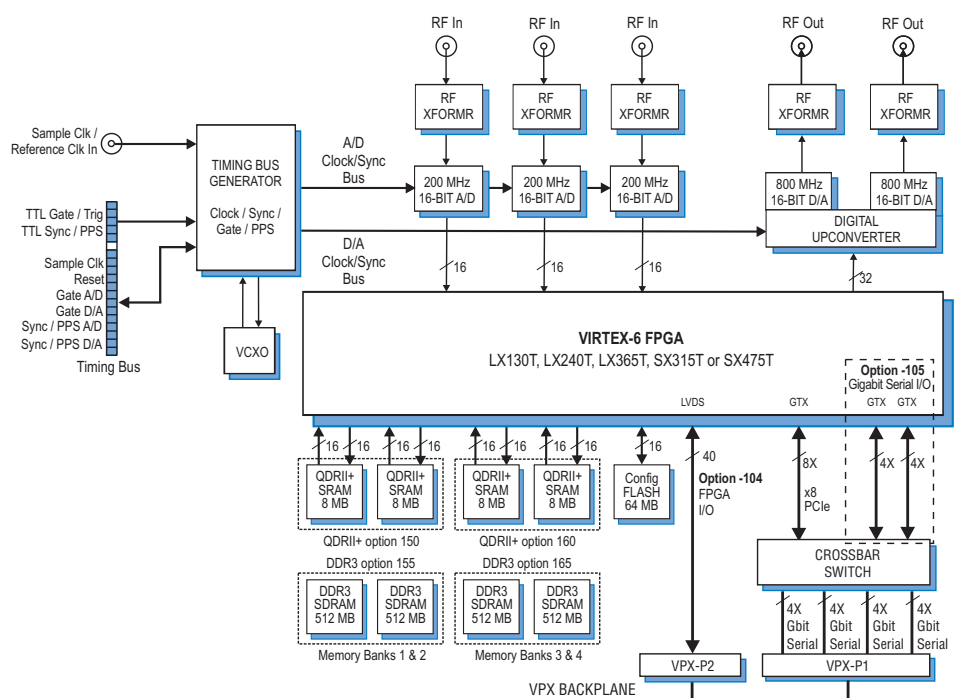
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



A/D Acquisition IP Modules

The 53620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TIDAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

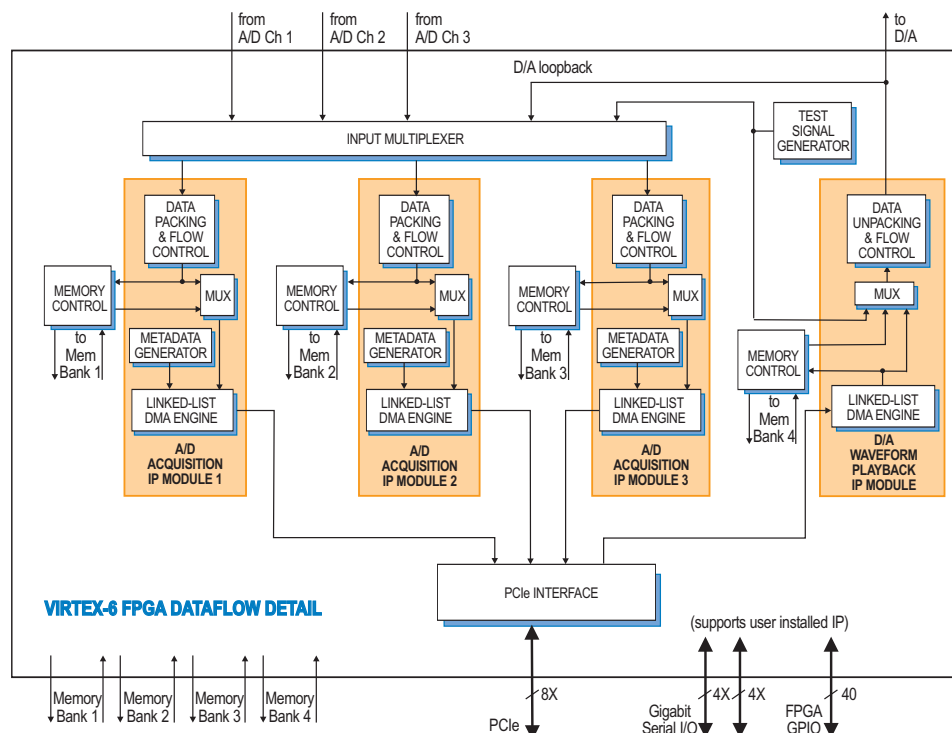
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



► board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

The 53620 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105: Provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI Express Interface

PCI Express Bus: Gen. 1 x8 or Gen.2 x4 over the 3U VPX backplane

Gigabit Serial I/O

VPX-P1: Four 4X ports to fabric-transparent crossbar switch

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model Description

53620 3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 3U VPX

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX



Model 53621 COTS (left)
and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53621 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53621 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53621 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition.

sition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

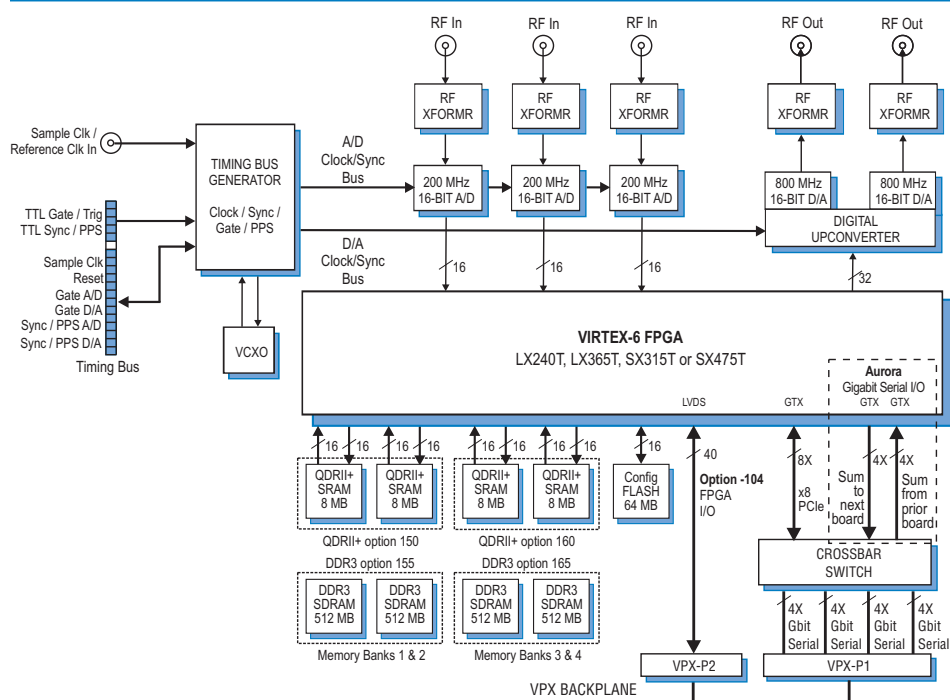
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



A/D Acquisition IP Modules

The 53621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency

setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Beamformer IP Core

In addition to the DDCs, the 53621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average

power level of any DDC core falls below or exceeds a programmable threshold.

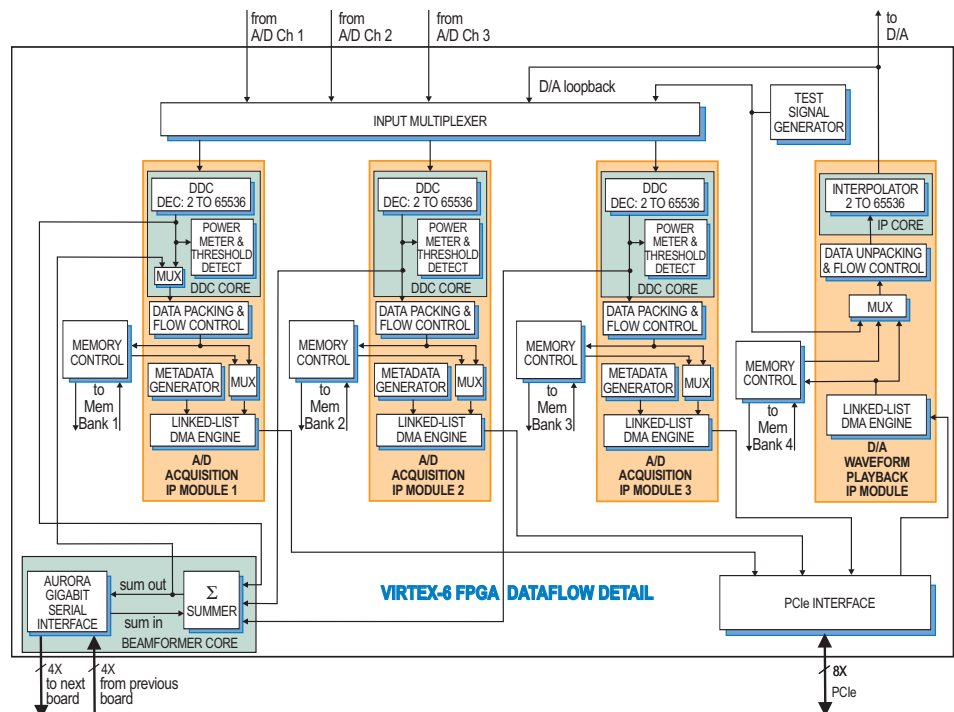
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



► A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TIDAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

The 53621 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X). ►

► Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Digital Downconverters

Quantity: Three channels

Decimation Range: 2 to 65,536 in integer steps

LO Tuning Freq. Resolution: 32 bits, 0 to Fs

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 2 Pi radians

FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Type: Texas Instruments DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 400 MHz max.

Output Signal: 2-channel real or 1-channel with frequency translation

Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation

Resolution: 16 bits

Digital Interpolator

Interpolation Range: 2x to 65,536 in integer steps

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or a 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4 over the 3U VPX backplane

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model Description

53621 3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U XMC

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 53630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX



Model 53630 COTS (left) and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53630 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 53630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the

factory-installed functions and enable the 53630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

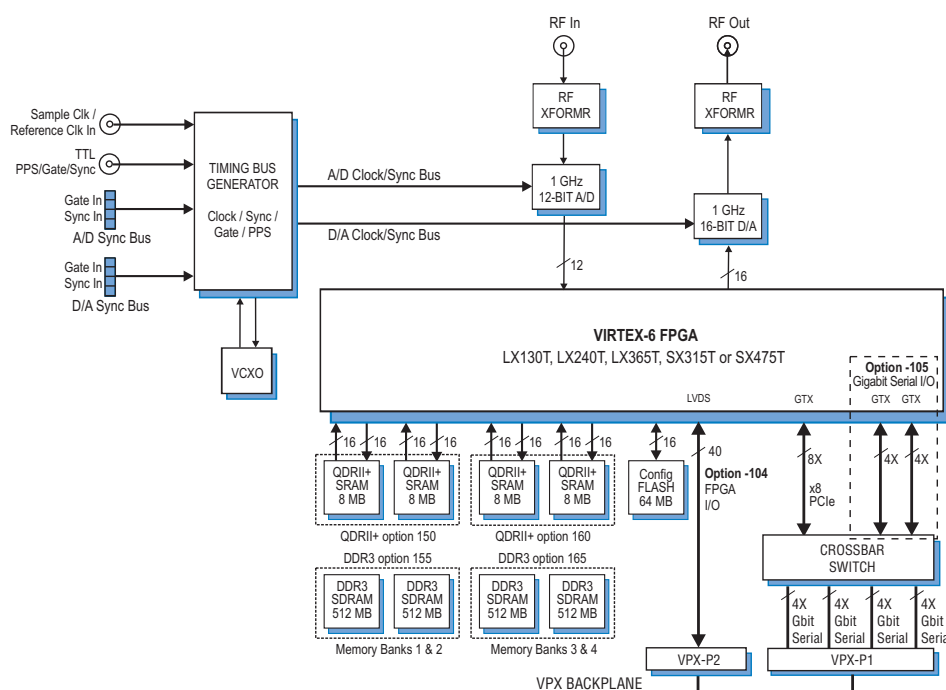
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



A/D Acquisition IP Module

The 53630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

► A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 53630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to pro-

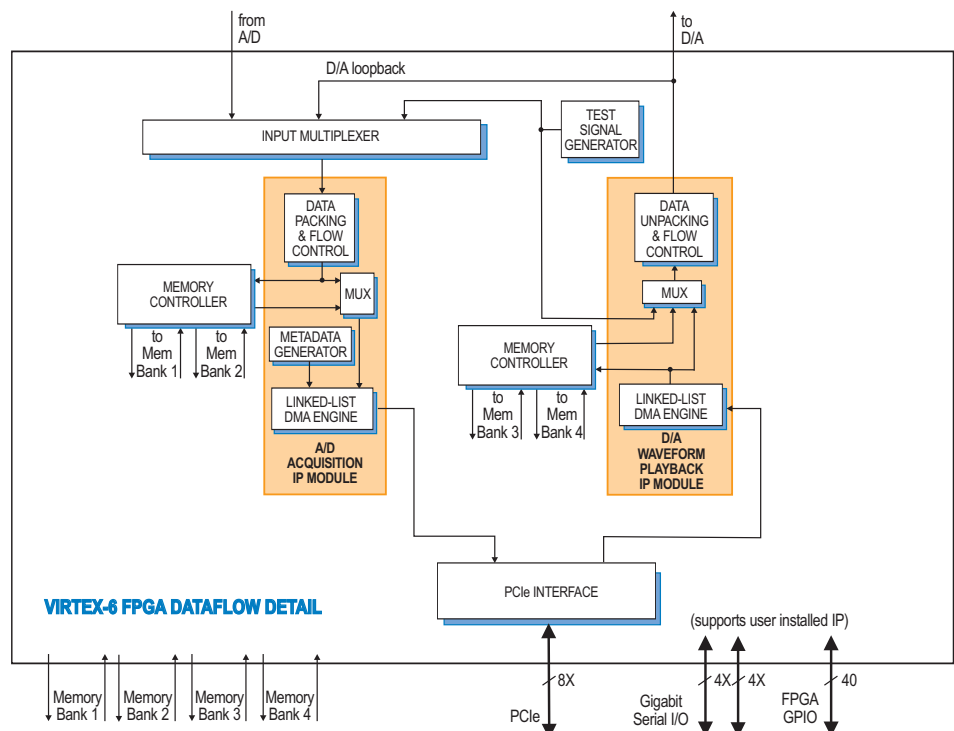
vide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Two front panel 7-pin LVPECL Sync connectors allow multiple boards to be synchronized. One connector for the A/D and one for the D/A each provide sync and gate signals.

Memory Resources

The 53630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ►



► Fabric-Transparent Crossbar Switch

The 53630 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts sample clock or a 5 or 10 MHz system reference

Timing Bus: 7-pin connectors, LVPECL bus for sync and gate, one A/D connector and one D/A connector

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105: Provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8 over the 3U VPX backplane

Gigabit Serial I/O

VPX-P1: Four 4X ports to fabric-transparent crossbar switch

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model Description

53630 1 GHz A/D and D/A,
Virtex-6 FPGA - 3U VPX

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 53650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX



Model 53650 COTS (left)
and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53650 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53650 includes two A/Ds, one DUC (digital upconverter), two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal

generator and a PCIe interface complete the factory-installed functions and enable the 53650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

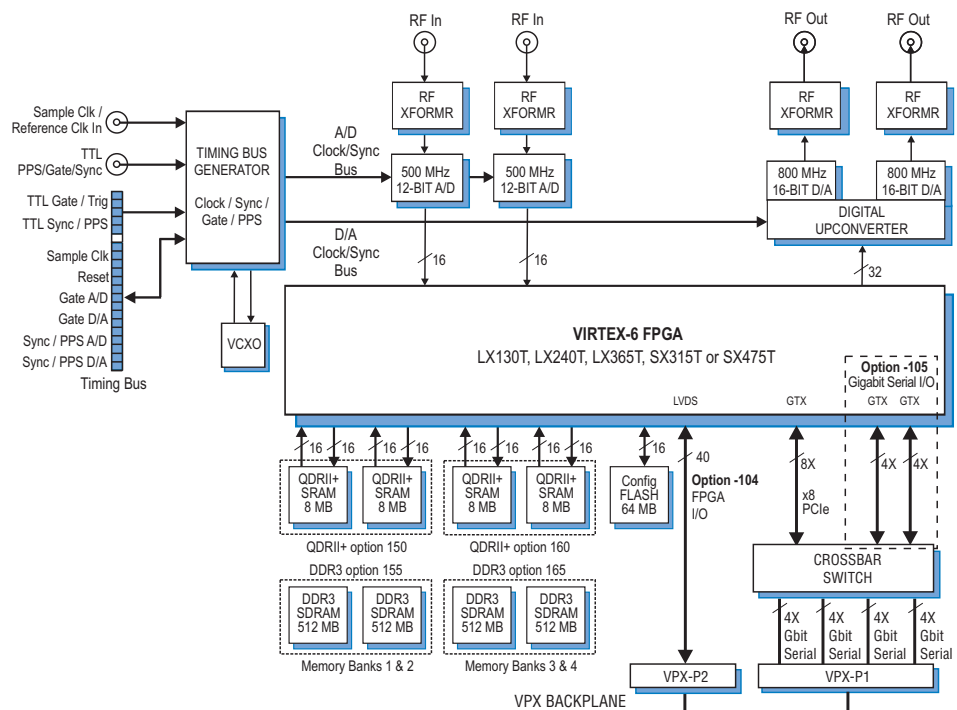
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



A/D Acquisition IP Modules

The 53650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

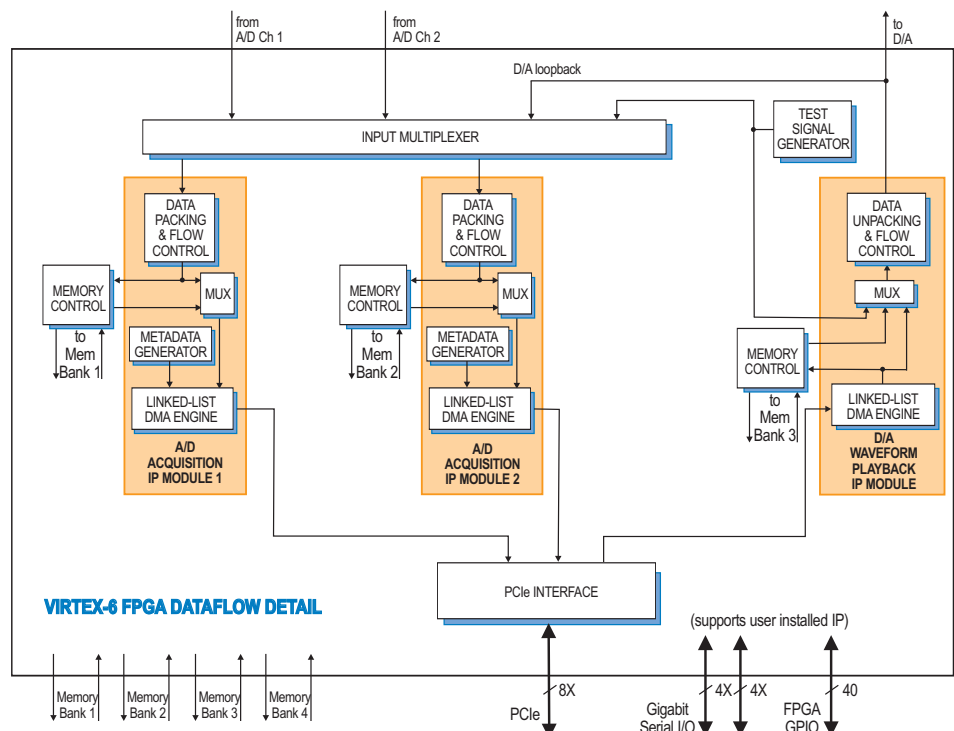
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the ➤



► board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

The 53620 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)

Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option 014)

Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

D/A Converters

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz, max.
Output IF: DC to 400 MHz, max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz, max. with interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 800 MHz sample clock or a 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VFX315T, or XC6VFX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105: Provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8 over the 3U VPX backplane

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;
 -20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model Description

53650 Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As with Virtex-6 FPGA - 3U VPX

Options:

-014 400 MHz, 14-bit A/Ds
 -062 XC6VLX240T
 -063 XC6VLX365T
 -064 XC6VFX315T
 -065 XC6VFX475T
 -104 LVDS FPGA I/O to VPX P2
 -105 Gigabit serial FPGA I/O to VPX P1
 -150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
 -160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
 -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
 -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 53660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX



Model 53660 COTS (left)
and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53660 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 53660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable

the 53660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

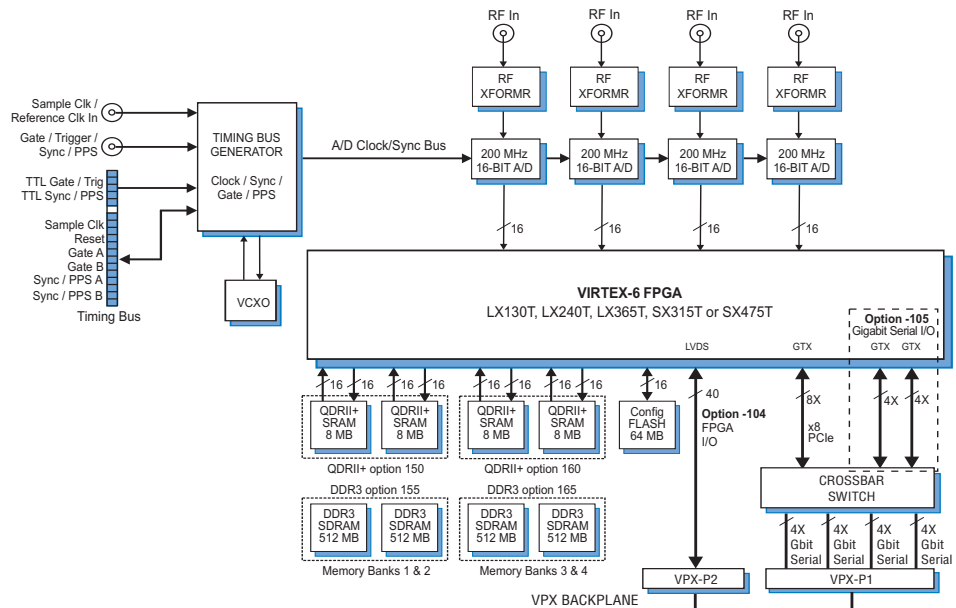
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



► A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

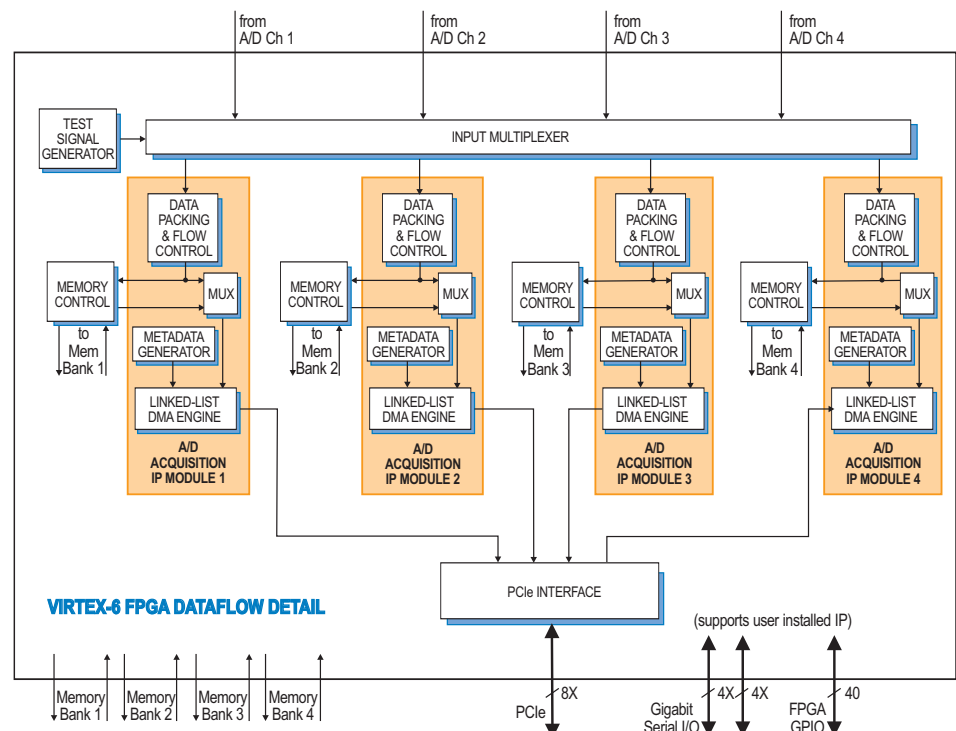
The 53660 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. ►

A/D Acquisition IP Modules

The 53660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105: Provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI Express Interface

PCI Express Bus: Gen. 1 x8 or Gen.2 x4 over the 3U VPX backplane

Gigabit Serial I/O

VPX-P1: Four 4X ports to fabric-transparent crossbar switch

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm).

Ordering Information

Model Description

53660 4-Channel 200 MHz,
16-bit A/D with Virtex-6
FPGA - 3U VPX

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 53661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX



Model 53661 COTS (left) and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53661 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53661 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchro-

nization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

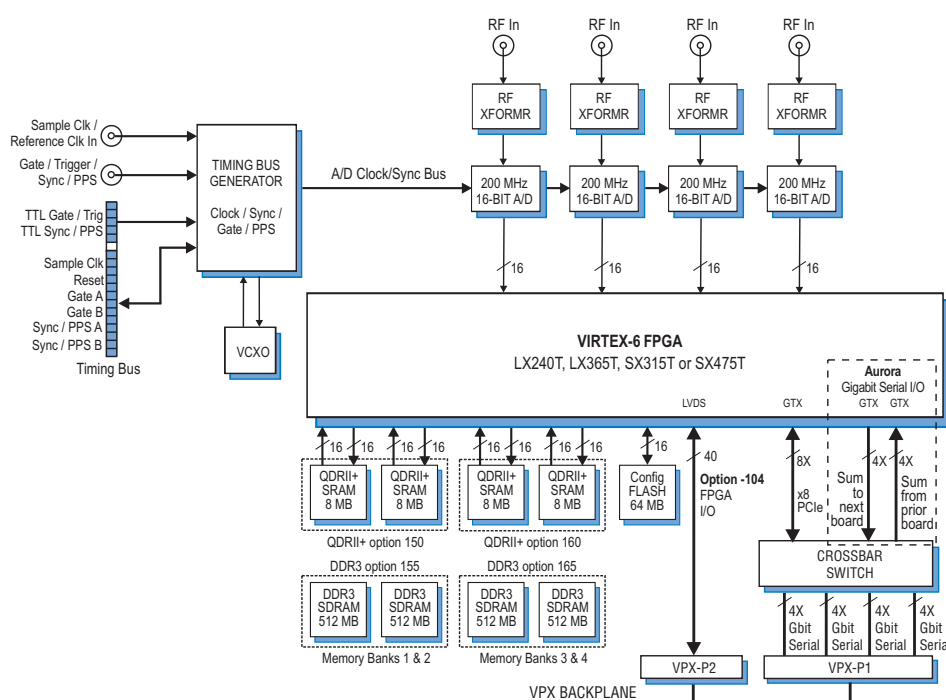
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, LX365T, SX315T, or SX475T.

The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ➤



A/D Acquisition IP Modules

The 53661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536

providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Beamformer IP Core

In addition to the DDCs, the 53661 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation

change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

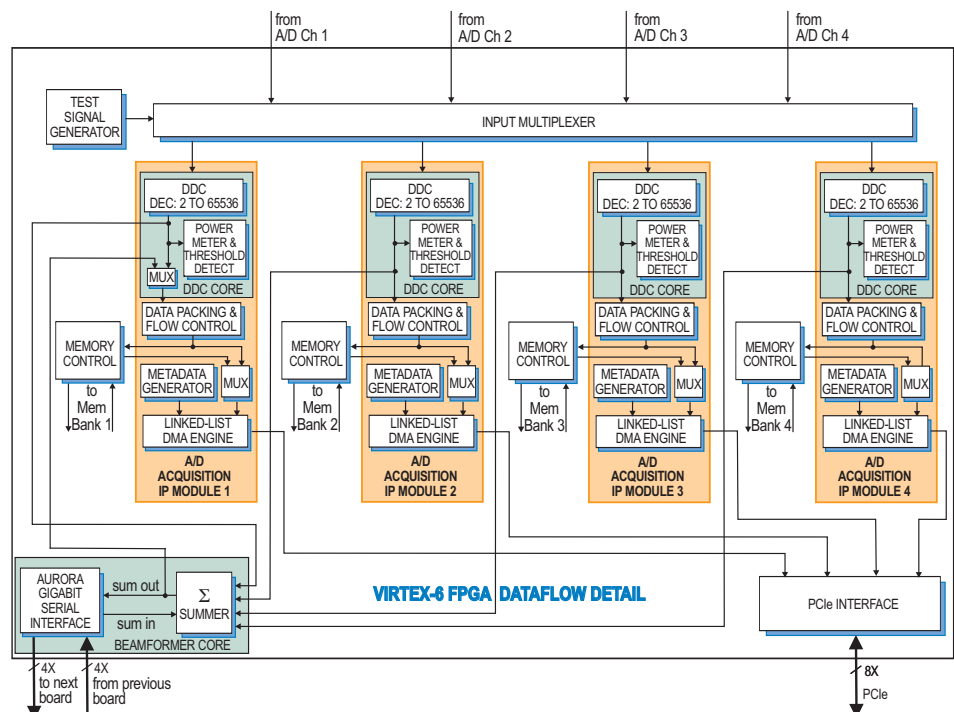
► A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage ►



► controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53661's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

The 53661 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Digital Downconverters

Quantity: Four channels

Decimation Range: 2 to 65,536 in integer steps

LO Tuning Freq. Resolution: 32 bits, 0 to Fs

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 2 Pi radians

FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms,

Function: 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4 over the 3U VPX backplane

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model Description

53661 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions



PENTEK

ANALOG & DIGITAL I/O

ANALOG & DIGITAL I/O

MODEL	DESCRIPTION
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC
7250, 7350	Quad or Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - cPCI
7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI
7750	Quad or Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x16 PCIe
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x8 PCIe
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX
Cobalt 71630	1 GHz A/D and D/A, Virtex-6 FPGA - XMC
Cobalt 78630	1 GHz A/D and D/A, Virtex-6 FPGA - Half-length PCIe
Cobalt 53630	1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX
Cobalt 71660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - XMC
Cobalt 78660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - Half-length PCIe
Cobalt 53660	4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX
6821, 6822	Single or Dual 215 MHz, 12-bit A/Ds with Virtex-II Pro FPGAs - VME/VXS
6826	Dual 2 GHz, 10-bit A/D with Virtex-II Pro FPGA - VME/VXS
6802	32-Channel A/D with FPDP Output - VME
6226	FPDP (Front Panel Data Port) Adapter - VIM-2
6236	14-bit A/D Converter with FPGA and Optional DDCs - VIM-2
6250	Configurable Logic FPGA with FPDP I/O - VIM-2
6251	Virtex-II Pro FPGA Configurable Logic and I/O - VIM-2
Customer Information	

[Click Here for the PRODUCT SELECTOR](#)

Last updated: November 2010

New!

Model 7150

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC



Features

- Complete software radio interface solution
- VITA 42.0 XMC compatible with switched fabric interfaces
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources ideally matched to the requirements of high-performance systems.

Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched-fabric interfaces.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The Model 7150 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters,

DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

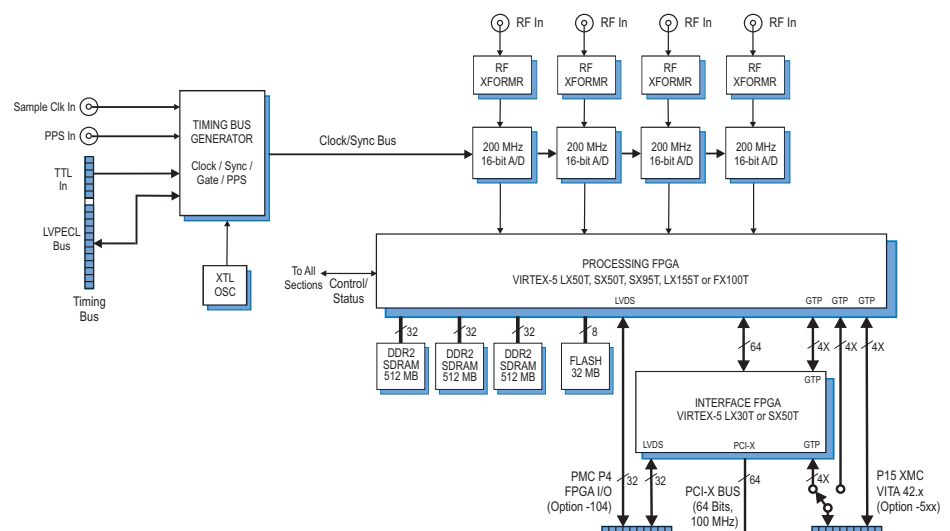
The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7150 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs the P4 PMC connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

The Model 7150 architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ➤



XMC Interface

The Model 7150 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides serial data links with up to 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7150 achieves up to 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7150s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. More modules can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI-X Interface

The Model 7150 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66, 100 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, the Model 7150 can be optionally factory-configured with x4 PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs P4 connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC
Options:	
-104	FPGA I/O through the P4 connector
-5xx	XMC interface

Contact Pentek for additional available options.

New!

Models 7250, 7250D and 7350

Quad or Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - cPCI



Model 7350 Model 7250D



Features

- Complete software radio interface solutions
- Four or eight 200 MHz, 16-bit A/Ds
- Up to 1.5 or 3.0 GB of DDR2 SDRAM
- Two or four Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Models 7250 and 7350 are cPCI Quad 200 MHz A/Ds. They consist of one Model 7150 Quad A/D mounted on a cPCI carrier. The Model 7250 is a 6U cPCI board, while the Model 7350 is a 3U cPCI board. Model 7250D is the same as the Model 7250, except it contains two 7150's rather than one.

A/D Converter Stage

The front end accepts four or eight full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into Xilinx Virtex-5 FPGAs for routing, formatting and DDC signal processing operations.

Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of

different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Models 7250 and 7350 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

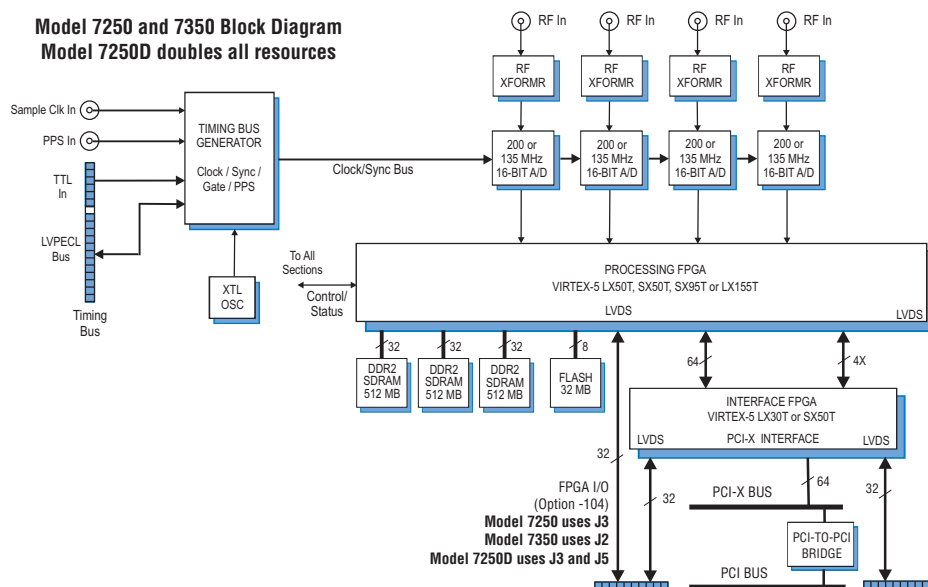
Option -104 installs the J3 connector (Model 7250) or the J2 connector (Model 7350) with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

With Model 7250D, the option provides an additional 16 pairs of LVDS connections through the J5 connector to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ➤

Model 7250 and 7350 Block Diagram
Model 7250D doubles all resources



► Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to two slave 7250Ds and three slave 7350s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

Both Models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33, and 66 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, these Models can be optionally factory-configured with x4 PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Specifications

Model 7250 or Model 7350: 4 A/Ds

Model 7250D: 8 A/Ds

Model 7250D shown in the Specifications Front Panel Analog Signal Inputs (8)

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources (4): Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clocks (4)

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPSinput/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array (4)

Processing FPGA: Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XCV5FX100T

Interface FPGA: Two Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs the J3 and J5 cPCI connectors with 32 pairs of LVDS connections to the processing FPGA and 32 pairs of LVDS connections to the interface FPGA for custom I/O

Memory

DDR2 SDRAM: Up to 3.0 GB in six banks

PCI Interface

PCI Bus: 32- or 64-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7250	Quad 200 MHz, 16-bit A/D with two Virtex-5 FPGAs - 6U cPCI
7250D	Octal 200 MHz, 16-bit A/D with four Virtex-5 FPGAs - 6U cPCI
7350	Quad 200 MHz, 16-bit A/D with two Virtex-5 FPGAs - 3U cPCI

Options:

-104	FPGA I/O through cPCI J3 for 7250 or J2 for 7350; cPCI J3 and J5 for 7250D

Contact Pentek for additional available options.

New!

Model 7650

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI



General Information

Model 7650 is a half-length PCI Quad 200 MHz A/D. It consists of one Model 7150 Quad A/D mounted on a PCI carrier board. The Model 7650 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA,

programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7650 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but additional processing resources up to an additional 640 DSP48E Slices.

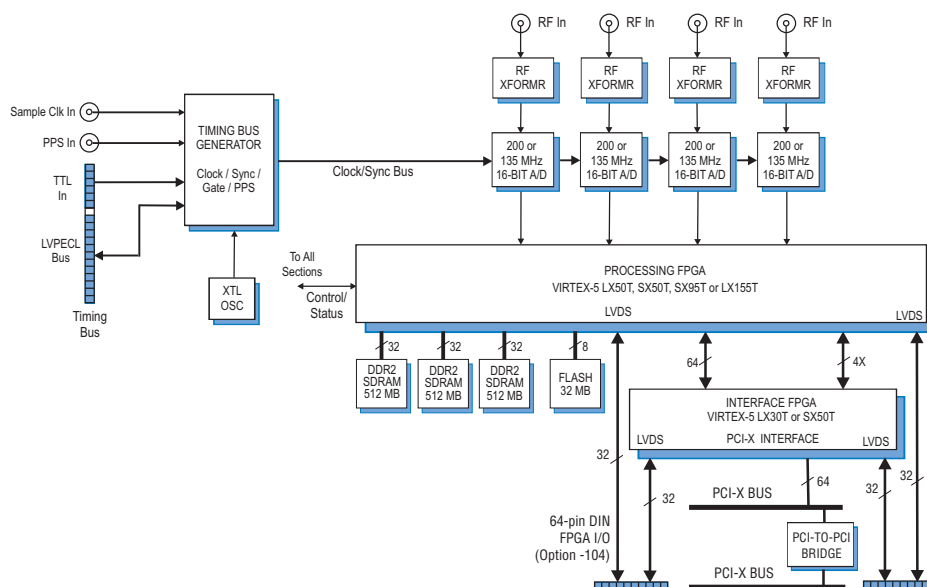
Option -104 installs a 64-pin DIN connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ➤

Features

- Complete software radio interface solution
- Four or 200 MHz, 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O



► Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI-X Interface

The Model 7650 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, the Model 7650 can be optionally factory-configured with x4 PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs a 64-pin DIN connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs to the interface FPGA for custom I/O

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI card

Ordering Information

Model	Description
7650	Quad 200 MHz, 16-bit A/D with two Virtex-5 FPGAs - PCI

Options:

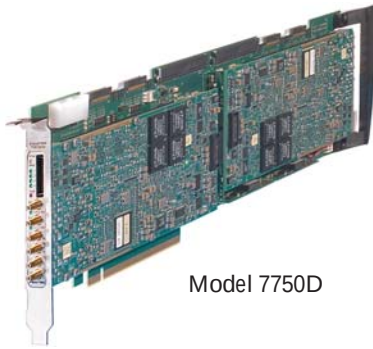
-104	FPGA I/O through a 64-pin DIN connector

Contact Pentek for additional available options.

New!

Models 7750, 7750D

Quad/Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x16 PCIe



Model 7750D



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Four or eight 200 MHz 16-bit A/Ds
- Up to 3 GB of DDR2 SDRAM
- Two or Four Xilinx Virtex-5 FPGAs
- Up to 5.12 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- Up to 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7750 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features either four 200 MHz, 16-bit A/Ds (Model 7750) or eight A/Ds (Model 7750D). These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 7750 attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

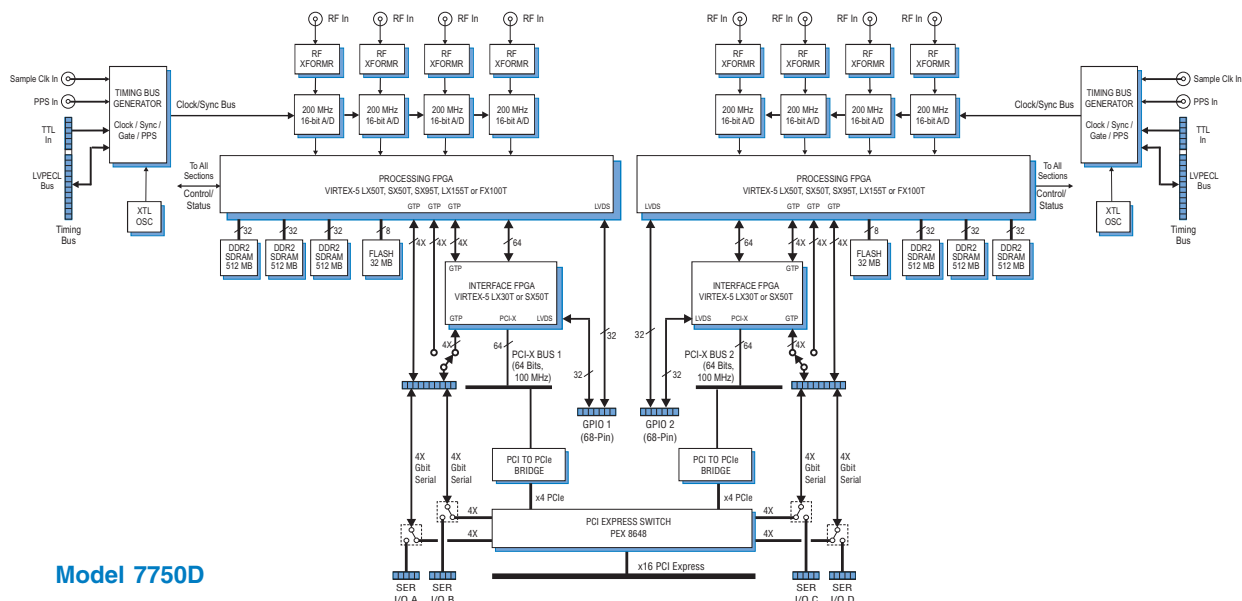
The Model 7750 architecture includes two (Model 7750) or four (Model 7750D) Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

There are two FPGA types on the 7750: processing and interface. The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, these Models can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express. Implementing the PCI interfaces in this FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to each processing FPGA, and 16 pairs of LVDS connections to each interface FPGA for custom I/O. ➤



Model 7750D

Clocking and Synchronization

The Model 7750 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7750s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to each processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7750 includes a multiple port, 48-lane Gen 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to each FPGA, as well as one x4 connection to each 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX50T (one for 7750, two for 7750D); optional FPGAs include:

XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: Xilinx Virtex-5 XC5VLX30T (one for 7750, two for 7750D); optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to each processing FPGA and 16 pairs to each interface FPGA

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks per processing FPGA (3 GB max.)

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x16 width

PCIe Ports: two x4 ports per FPGA

one x4 port per PCI bus

one x16 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.

Ordering Information

Model	Description
7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length x16 PCIe
7750D	Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length x16 PCIe
Options:	
-104	FPGA I/O through the GPIO connector(s)
-5xx	Gigabit Serial I/O - two full duplex 4X paths (Model 7750) or four full duplex 4X paths (Model 7750D)

Contact Pentek for additional available options.

New!

Model 7850

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x8 PCIe



Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- Up to 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7850 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds. These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 7850 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The Model 7850 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

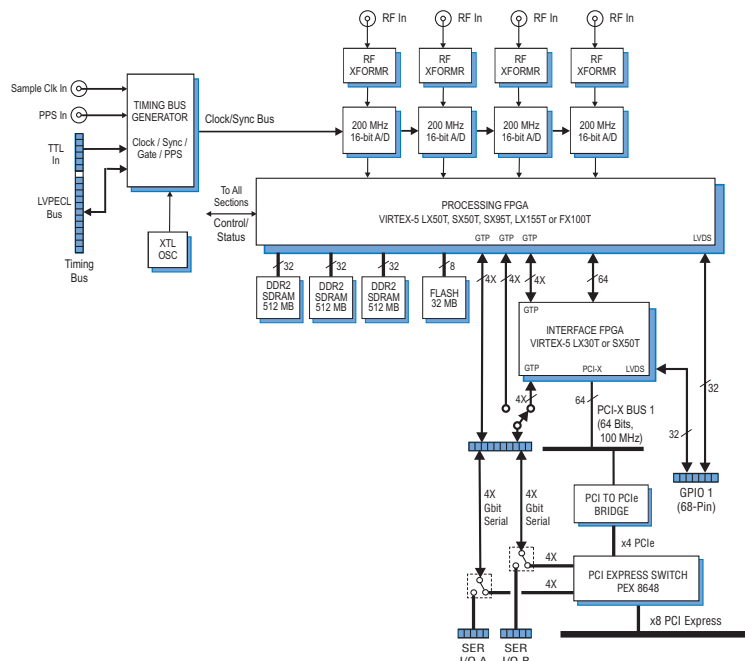
There are two FPGA types on the 7850: processing and interface. The pro-

cessing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7150 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express. Implementing the PCI interfaces in this FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O. ➤



Clocking and Synchronization

The Model 7850 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7850s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7850 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to the processing FPGA, as well as one x4 connection to the 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5

XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: Xilinx Virtex-5

XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Provides GPIO with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

PCIe Interface: Gen. 2, x8 width

PCIe Ports: two x4 ports to processing FPGA; one can be alternately routed to interface FPGA

one x4 port to PCI bus

one x8 port to PCIe motherboard

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Half-length x8 PCIe
Options:	
-104	FPGA I/O through the GPIO connector(s)
-5xx	Gigabit Serial I/O - two full duplex 4X paths

Contact Pentek for additional available options.

New!

Model 5350

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX



Model 5350 commercial (left) and conduction-cooled version



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- Up to 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
VITA-46 (VPX Baseline Standard)
VITA-48 (VPX REDI)
VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 5350 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds. These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 5350 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other board resources.

Virtex-5 FPGAs

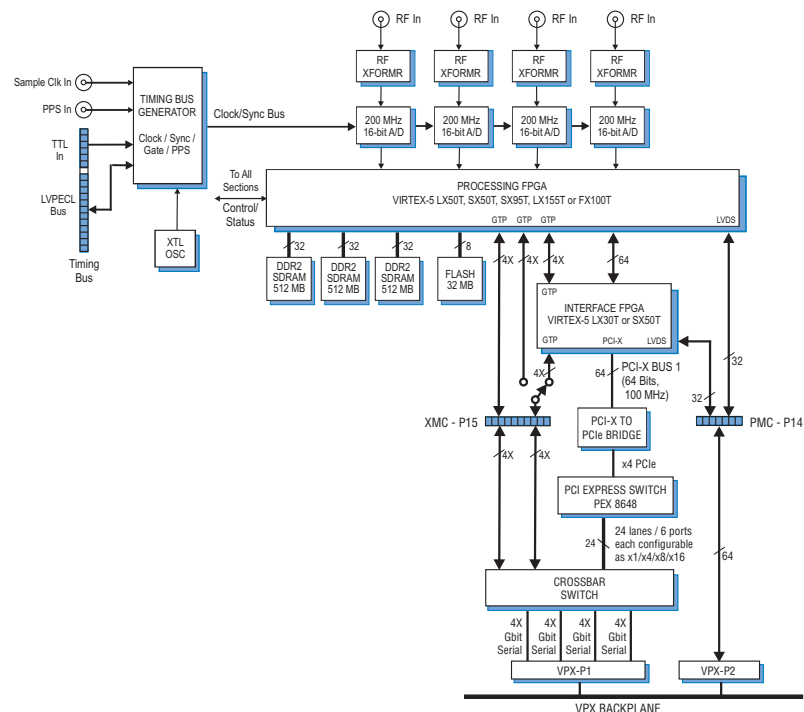
The Model 5350 architecture includes two Virtex-5 FPGAs. All data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP.

There are two FPGA types on the 5350: processing and interface. The processing FPGA serves as a control and status engine with data and programming interfaces to each of the onboard resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 5350 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express, preserving the processing FPGA resources for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O. ➤



Clocking and Synchronization

The Model 5350 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 5350s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Two of the banks support built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. These banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of all three banks to support various applications.

Fabric-Transparent Crossbar Switch

The 5350 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

PCI Express Switch

Model 5350 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: Xilinx Virtex-5 XC5VSX50T standard; XC5VLX50T, XC5VSX95T, XC5VLX155T or XC5VFX100T, optional

Interface FPGA: Xilinx Virtex-5 XC5VLX30T std.; XC5VSX50T optional

Custom I/O

Option -104: Provides GPIO to VPX-P2 with 16 LVDS pairs to processing FPGA (SX95T, LX155T or FX100T only) and 16 pairs to interface FPGA

Memory

DDR2 SDRAM: to 1.5 GB in three banks

PCI to PCIe Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

Processing FPGA: Two 4X ports to Fabric-Transparent Switch; one can be alternately routed to interface FPGA

VPX-P1: Four 4X ports to Fabric-Transparent Crossbar Switch

PCI Express: Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental

Operating Temperature:

Forced-Air Cooled: 0° to 50° C std;
-20° to 65° C (Level L2)

Conduction-Cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX
Options:	
-104	FPGA I/O to VPX-P2
-5xx	Gigabit Serial I/O to VPX-P1- four full duplex 4X paths
-703	Level L3 Conduction-Cooled Version

Contact Pentek for additional available options.

New!

Model 71630

1 GHz A/D and D/A, Virtex-6 FPGA - XMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71630 is a member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71630 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 71630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking

and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

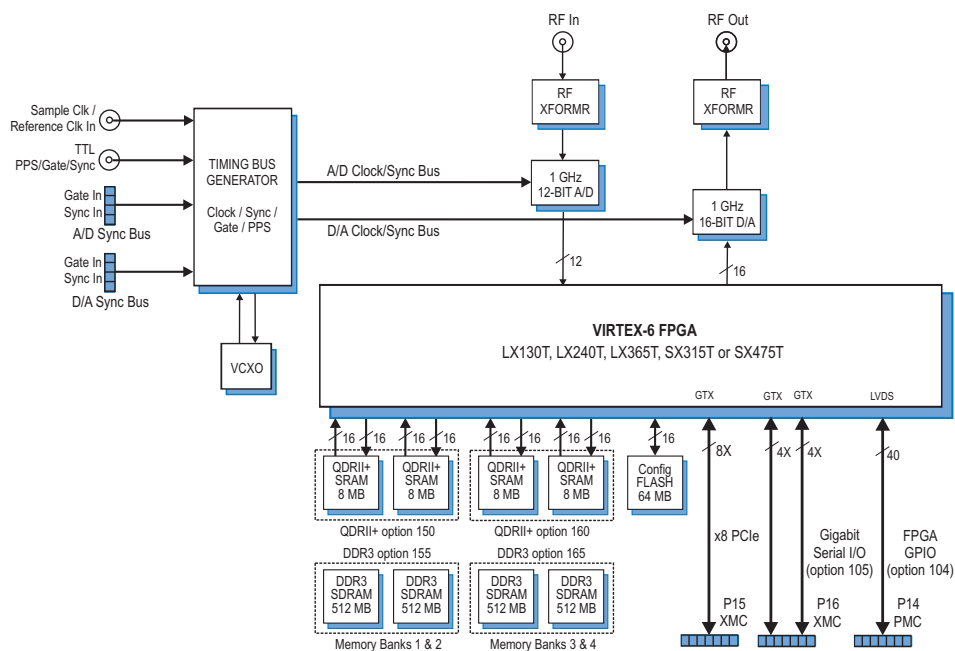
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. ➤



A/D Acquisition IP Module

The 71630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 71630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to pro-

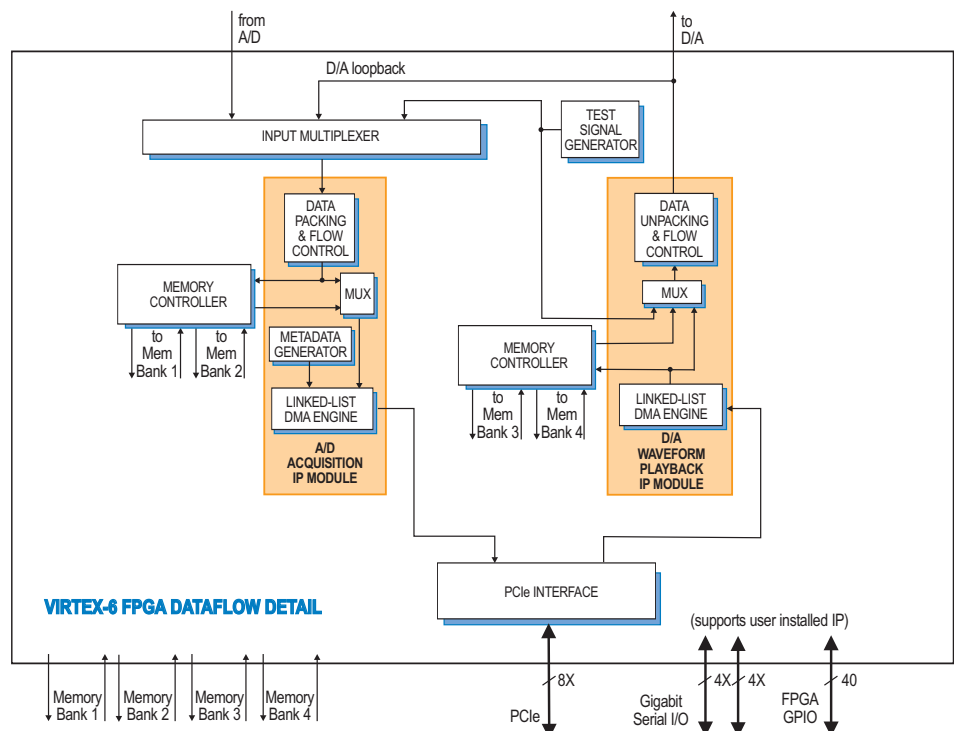
vide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Two front panel 7-pin LVPECL Sync connectors allows multiple modules to be synchronized. One connector for the A/D and one for the D/A each provide sync and gate signals.

Memory Resources

The 71630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



► XMC Interface

The Model 71630 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71620 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts sample clock or a 5 or 10 MHz system reference

Timing Bus: 7-pin connectors, LVPECL bus for sync and gate, one A/D connector and one D/A connector

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71630 1 GHz A/D and D/A,
Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 78630

1 GHz A/D and D/A, Virtex-6 FPGA - x8 PCIe



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78630 is a member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking

and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

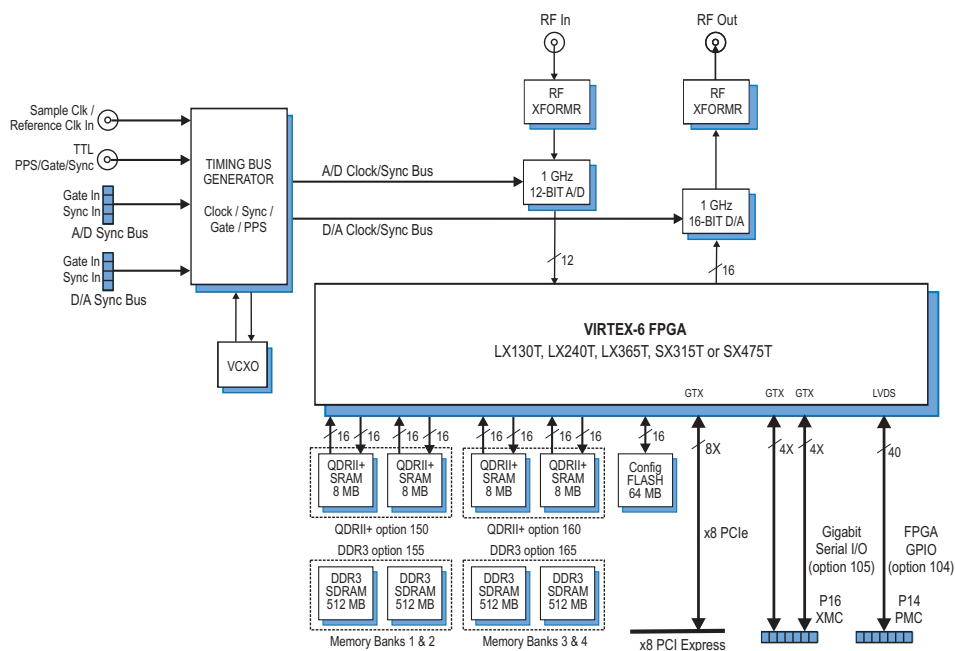
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. ➤



A/D Acquisition IP Module

The 78630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

D/A Converter Stage

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided

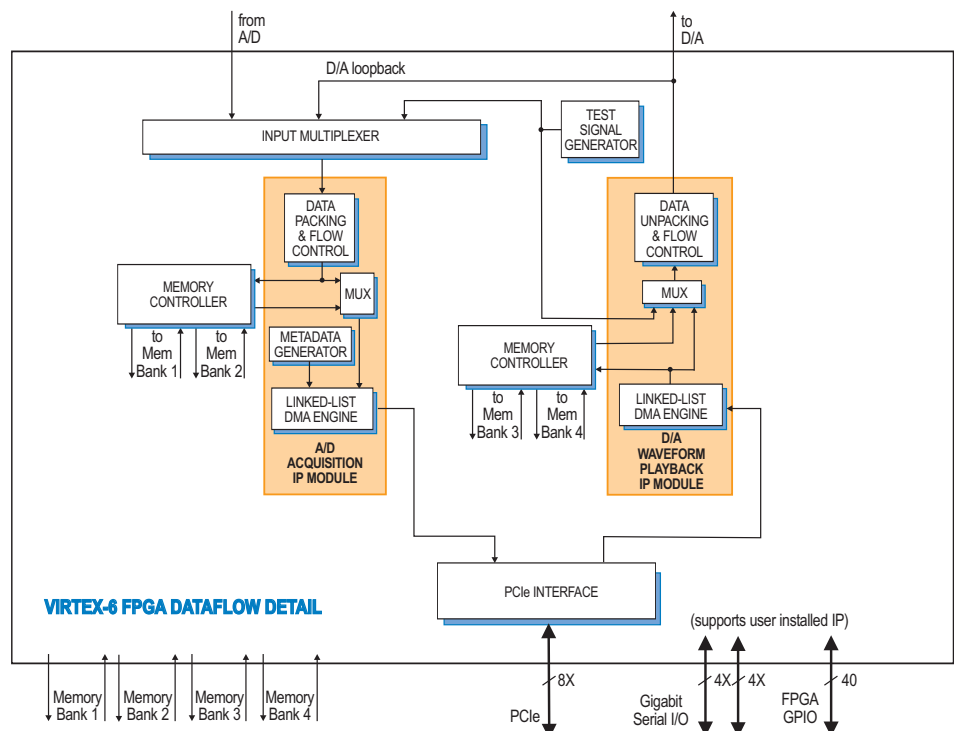
by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Two front panel 7-pin LVPECL Sync connectors allow multiple boards to be synchronized. One connector for the A/D and one for the D/A each provide sync and gate signals.

Memory Resources

The 78630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



► PCI Express Interface

The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts sample clock or a 5 or 10 MHz system reference

Timing Bus: 7-pin connectors, LVPECL bus for sync and gate, one A/D connector and one D/A connector

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78630 1 GHz A/D and D/A,
Virtex-6 FPGA - x8 PCIe

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 53630

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX



Model 53630 COTS (left)
and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53630 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 53630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the

factory-installed functions and enable the 53630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

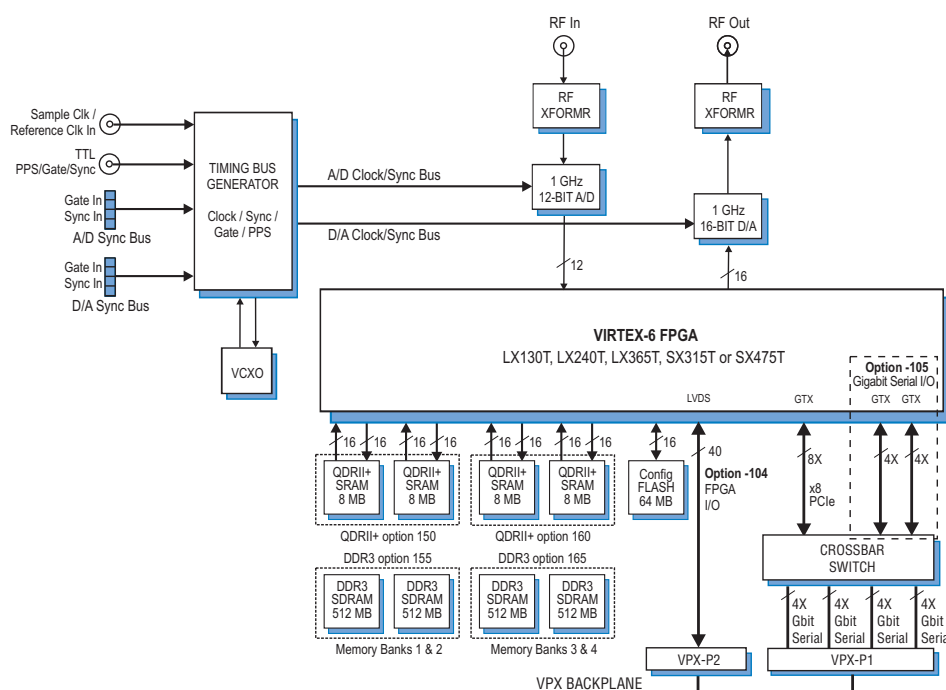
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



A/D Acquisition IP Module

The 53630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

► A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 53630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to pro-

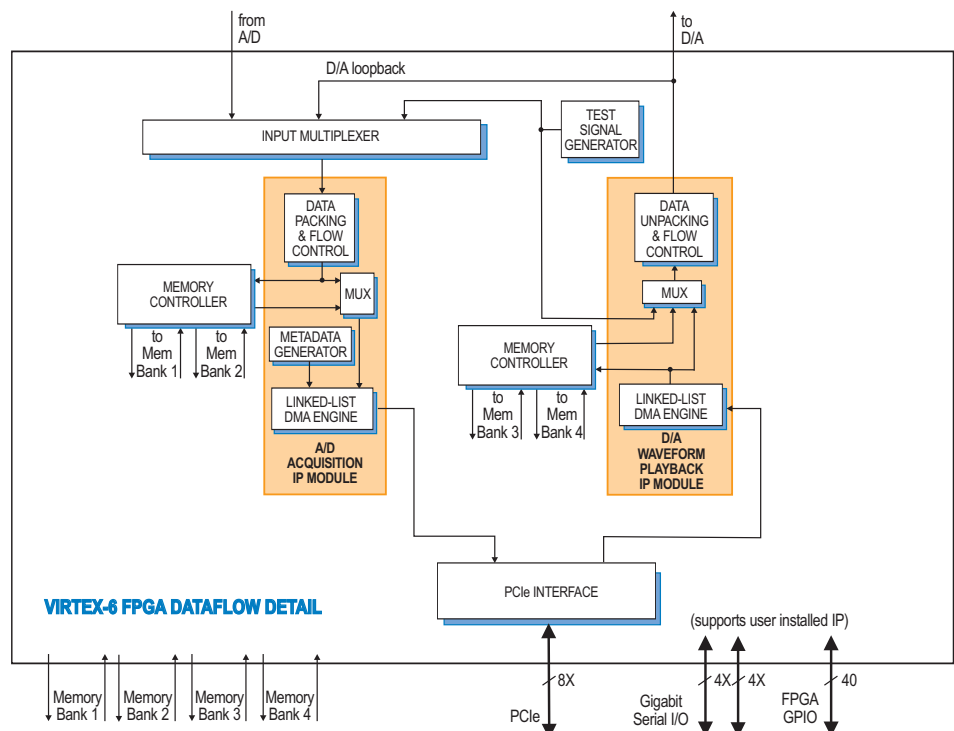
vide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Two front panel 7-pin LVPECL Sync connectors allow multiple boards to be synchronized. One connector for the A/D and one for the D/A each provide sync and gate signals.

Memory Resources

The 53630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ►



► Fabric-Transparent Crossbar Switch

The 53630 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts sample clock or a 5 or 10 MHz system reference

Timing Bus: 7-pin connectors, LVPECL bus for sync and gate, one A/D connector and one D/A connector

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105: Provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen.1 or Gen.2, x4 or x8 over the 3U VPX backplane

Gigabit Serial I/O

VPX-P1: Four 4X ports to fabric-transparent crossbar switch

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;

-20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model Description

53630 1 GHz A/D and D/A,
Virtex-6 FPGA - 3U VPX

Options:

-062	XC6VLX240T
-063	XC6VLX365T
-064	XC6VSX315T
-065	XC6VSX475T
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 71660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - XMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- User-configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71660 is the second member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal

generator, and a PCIe interface complete the factory-installed functions and enable the 71660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

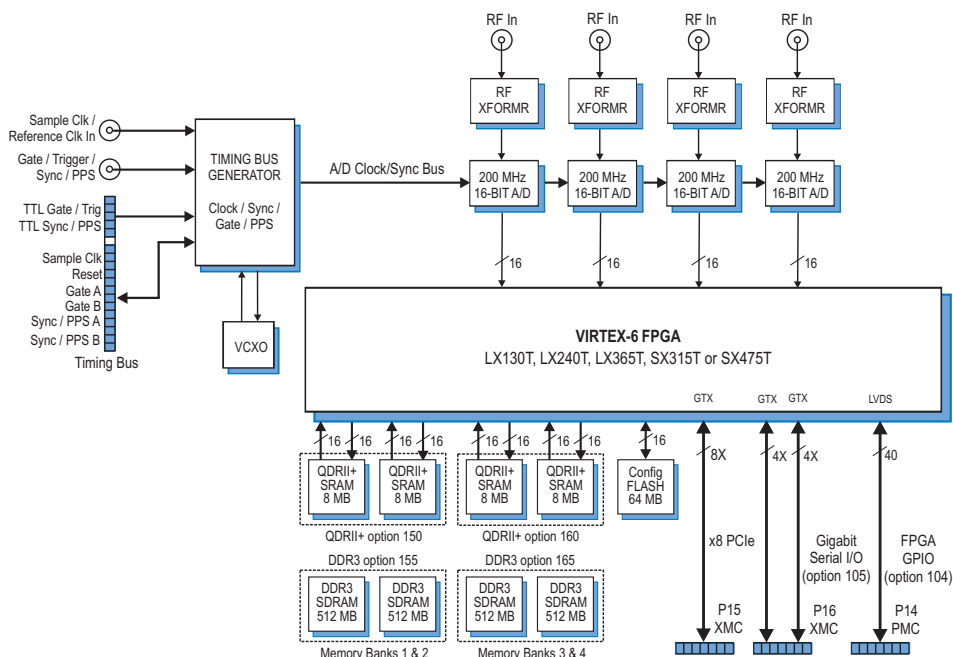
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤



► A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

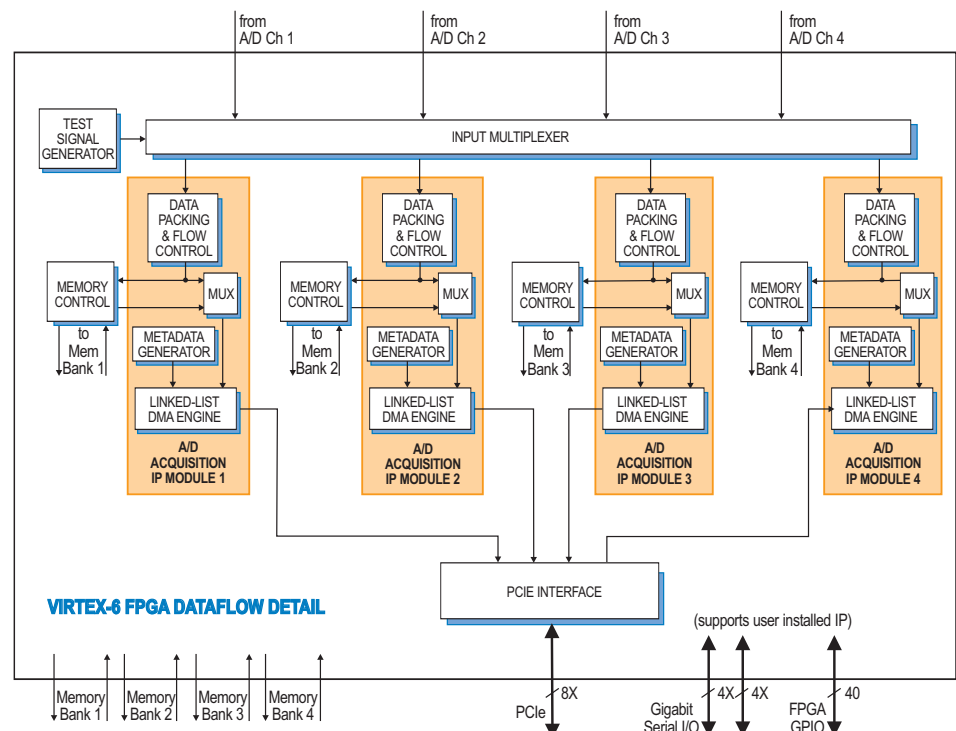
The Model 71660 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71660 ►

A/D Acquisition IP Modules

The 71660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description

71660 4-Channel 200 MHz A/D with Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

New!

Model 78660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - x8 PCIe



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- User-configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 78660 is the second member of the Cobalt™ family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board's analog interfaces. The 78660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal

generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

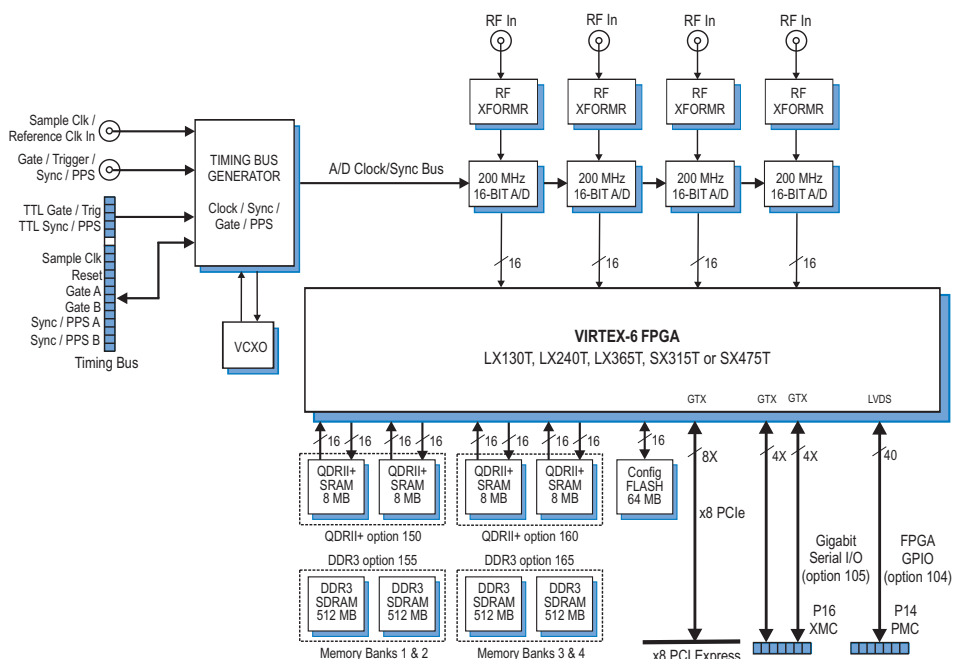
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Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤



► A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

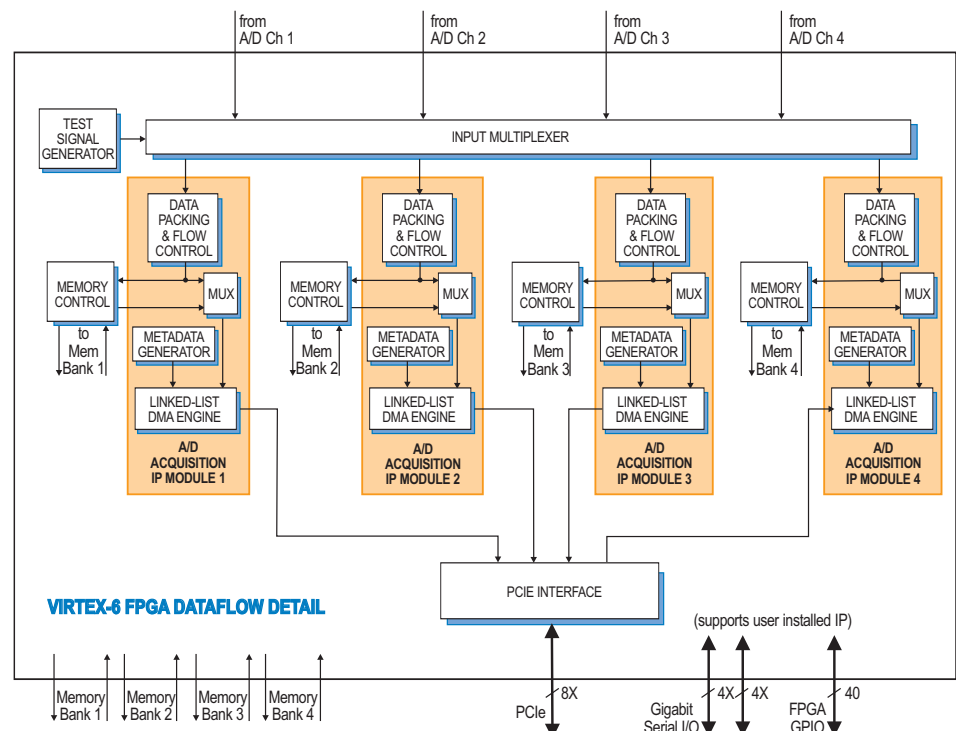
The Model 78660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board. ►

A/D Acquisition IP Modules

The 71660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms,

Function: accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen. 2 x4

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model Description

78620 4-Channel 200 MHz A/D with Virtex-6 FPGA - PCIe

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

Rev. 0702

PENTEK

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New!

Model 53660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX



Model 53660 COTS (left)
and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53660 is a member of the Cobalt™ family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 53660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable

the 53660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

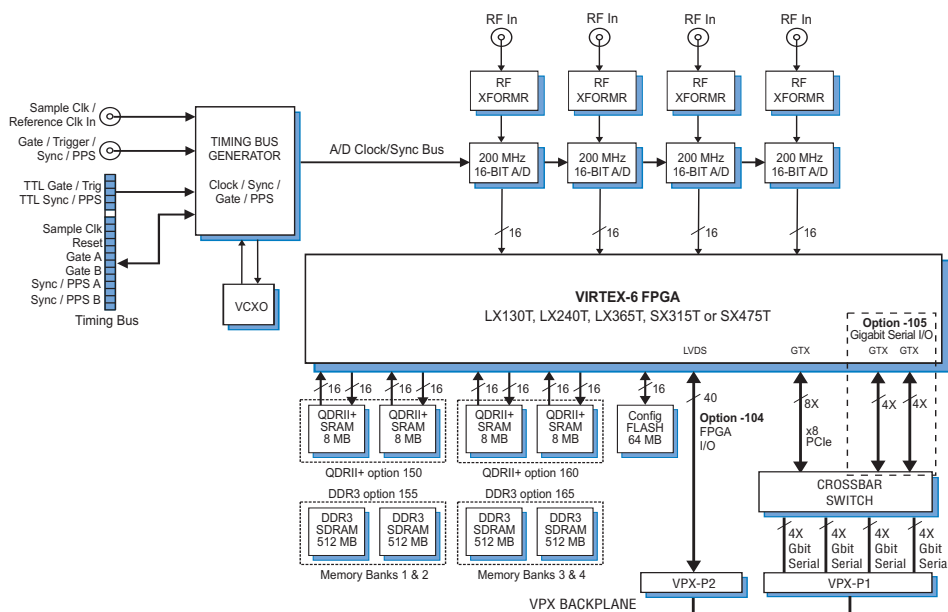
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



► A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Fabric-Transparent Crossbar Switch

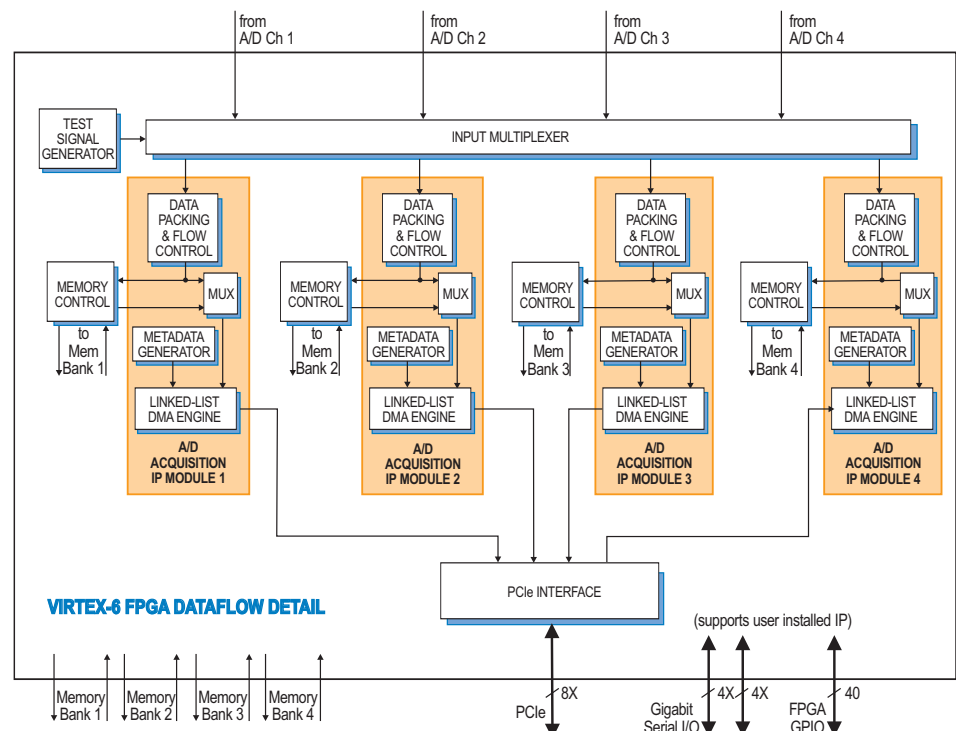
The 53660 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. ►

A/D Acquisition IP Modules

The 53660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus
Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 500 MHz sample clock or 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105: Provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks

PCI Express Interface

PCI Express Bus: Gen. 1 x8 or Gen.2 x4 over the 3U VPX backplane

Gigabit Serial I/O

VPX-P1: Four 4X ports to fabric-transparent crossbar switch

Environmental

Operating Temperature:

Forced-air cooled: 0° to 50° C std;
 -20° to 65° C (Level L2)

Conduction-cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm).

Ordering Information

Model Description

53660 4-Channel 200 MHz,
 16-bit A/D with Virtex-6
 FPGA - 3U VPX

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions



Model 6822 standard single slot (left)
and conduction-cooled version.



General Information

Models 6821 (single-channel) and 6822 (dual-channel) are complete high-frequency A/D converters in a 6U VMEbus form factor. They accept one or two front panel analog inputs and deliver digital output samples over two or four FPDP ports utilizing FPDP or FPDP II standards. These Models are ideal as high-speed data acquisition front ends for real-time recording, digital receivers, and DSP systems.

Input Stage and A/D Converters

Front panel female SMA connectors accept analog RF inputs at a full scale level of +8 dBm or +2 dBm (software selectable) into the primary of RF transformers that present 50 ohm input impedance. The transformers offer low-distortion paths to the differential inputs of the Analog Devices AD9430 A/Ds, with flat frequency response from 400 kHz to 700 MHz (standard).

Clocking, Gating and Triggering

The A/D converter sample clock can be sourced from an internal 210 MHz crystal oscillator or from an externally supplied sinusoidal clock of 215 MHz, maximum. This clock is accepted through a front panel SMA connector terminated in 50 ohms.

An external LVDS bus supports synchronous data acquisition across multiple boards. This is ideal for applications such as multichannel radar systems.

Virtex-II Pro FPGAs

Both Models utilize two Xilinx Virtex-II Pro Series FPGAs. Each FPGA is optionally

equipped with 128 MB of SDRAM and 16 MB of FLASH memory.

Each FPGA accepts 12-bit signals at the sampling frequency from the A/D converter. Several data packing modes are selectable across the multiple FPDP ports. The FPGAs also act as controllers for other board functions including gating and triggering.

Optional LVDS I/O is available through either the VMEbus P2 connector or a second-slot front panel mezzanine.

FIFOs and FPDP Outputs

Following each FPGA are two 32-bit wide FIFO buffers with standard depth of 32k words. These FIFOs are useful as elastic memory to support hard disk latencies in recording applications.

A total of four FPDP output ports are available, two per FPGA, to support data transfers of 320 MB/sec each or greater.

One port per FPGA is attached to the board's front panel, with the second attached to an optional second-slot front panel.

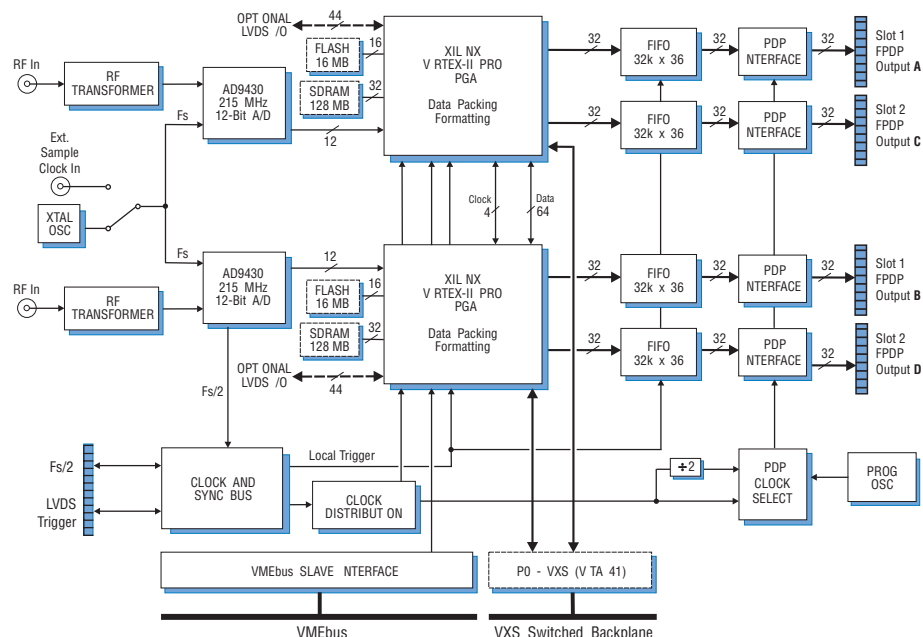
A data demultiplexing mode splits the data stream between each pair of FPDP ports, reducing the output data rate by a factor of up to four (depending on the data packing mode and number of FPDP ports) to support slower FPDP devices.

Optional VXS Interface

Both Models provide optional full duplex VITA-41 VXS links to the VME P0 connector for both FPGAs. These links support 4X Serial RapidIO, or other switched fabrics such as PCI Express and Xilinx Aurora. ➤

Features

- One or two AD9430 12-bit, 215 MHz A/D converters
- Xilinx Virtex-II Pro FPGAs
- Dual 4X VXS links for Serial RapidIO
- I/F input up to 700 MHz
- Four FPDP or FPDP II front panel ports
- FIFO data buffering
- Multiboard synchronization
- **Ruggedized and conduction-cooled versions available**



► Switchless VXS Card Cage

A five-slot card cage with full fabric support for three payload cards without the need for a switch card is now available for developing and testing VXS cards.

Specifications

Front Panel Analog Signal Inputs

Quantity: Model 6821: 1, Model 6822: 2
Input Type: Transformer-coupled, front panel female SMA connector
Full Scale Input: +8 dBm (1.59 V p-p) or +2 dBm (0.796 V p-p), software selectable, into 50 ohms
Input Bandwidth: 150 MHz
Transformer 3 dB Passband: 400 kHz to 700 MHz (other values optionally available)

A/D Converter

Quantity: Model 6821: 1, Model 6822: 2
Type: Analog Devices AD9430-210
Sampling Rate: 60 MHz to 215 MHz
Internal Clock: 210 MHz crystal osc. std.; 213.333 MHz crystal osc. optional
External Clock: 60 to 215 MHz
Resolution: 12 bits
Bandwidth: 700 MHz at full power

Clock Source: Onboard crystal oscillator, front panel external clock

External Clock: Front panel female SMA connector, sine wave, 0 to +4 dBm, AC coupled, 50 ohms impedance

Sync/Gate Bus: One 26-pin connector with one clock, one FPGA sync, and four gate input/output LVDS signals; one sync and one gate input TTL signals

Field Programmable Gate Arrays

Quantity: 2, both Models

Type:

Option -050: Virtex-II Pro XC2VP50-5

Option -020: Virtex-II Pro XC2VP20-5

FPGA I/O:

Option -222: Adds one 68-pin connector per FPGA through a second-slot front panel; each connector provides thirty two LVDS data I/O differential pairs, two LVDS clock I/O pairs and four control I/O pairs

Option -121: Provides twenty four LVDS differential data I/O pairs, two clock I/O pairs and four control pairs from FPGA2 to VMEbus P2 connector (not available with XC2VP20)

Memory

SDRAM:

Quantity: 2 banks, 1 per FPGA
Size: 128 MB per bank (256 MB total)
Bus Width: 32 bits
Speed: 133 MHz

FLASH:

Quantity: 2, 1 per FPGA

Size: 16 MB each (32 MB total)

Bus Width: 16 bits

Front Panel Data Port (FPDP) Outputs

Quantity: 2 standard; 4 with option

-224 (additional ports located on second-slot front panel)

Output Type: non-inverted configuration, FPDP I or FPDP II

Clock: Onboard programmable oscillator (up to 50 MHz), or sample clock with one line to each FPDP port

FIFOs

Quantity: 2 standard (one per FPDP port), 4 with option -224

Size: 32,768 x 36

Speed: Sample clock rate ÷ 2

VME Slave Interface

Type: Slave A16/D16, A16/D32 (A32/D32 programmable)

Control: Operating modes, gate/trigger, FIFO reset, data packing, FPDP I/II selection, FPDP framing, time sync command, status

Power

Default Configuration: 19 W

Note: User FPGA designs will increase power consumption, normally within the following ranges:

With XC2VP20 FPGAs: from 28 W to 38 W maximum

With XC2VP50 FPGAs: from 41 W to 62 W maximum

Environmental (Commercial version)

Pentek Ruggedization Level: L0

Cooling Method: Forced air

Operating Temp: 0 to 50° C

Storage Temp: -20 to 90° C

Relative Humidity: 0 to 95%, non-condensing

Environmental - Option -703

Pentek Ruggedization Level: L3

Cooling Method: Conduction cooling

Operating Temp: -40 to 70° C

Storage Temp: -50 to 100° C

Relative Humidity: 0 to 95%, non-condensing

Sine Vibration: 10 g, 20-2,000 Hz

Random Vibration:

0.1 g²/Hz, 20-2,000 Hz

Shock: 30 g, 11 ms

Environmental - Option -720

Relative Humidity: 0 to 100% non-condensing with conformal coating

Size: Standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 20.3 mm (0.8 in) wide; Option -222 or -224: 40.6 mm (1.6 in) wide

Weight: 425 grams (15 oz.); 794 grams (28 oz.) conduction-cooled version

Ordering Information

Model	Description
6821	Single 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS
6822	Dual 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS
Options:	
-020	XC2VP20 FPGAs
-050	XC2VP50 FPGAs
-121	LVDS I/O thru P2
-213	213.333 MHz crystal oscillator
-222	2nd Slot LVDS I/O
-224	2nd Slot FPDP I/O
-234	FPDP for conduction-cooled version
-340	128 MB SDRAM and 16 MB FLASH per FPGA
-422*	Wideband Ultra High-Speed DDC IP Core factory-installed
-5xx	VXS Interface
-70x	Ruggedized & conduction-cooled versions

* See Section 1 for more information



Features

- One or two 10-bit, 2 GHz A/D converters
- Xilinx Virtex-II Pro FPGA
- Dual 4X full duplex VXS links
- Two or four front panel FPDP or FPDP II outputs
- Up to 1 GB DDR SDRAM
- Multiboard synchronization: up to eight dual-channel 6826's may be synchronized with the Model 6890 clock, sync and gate distribution board
- **Ruggedized and conduction-cooled versions available**

General Information

The Model 6826 is a high-frequency single or dual channel A/D converter in a 6U VMEbus form factor. It accepts one or two front panel analog inputs and delivers digital output samples over two or four FPDP connectors utilizing FPDP or FPDP II standards. The 6826 is an ideal high-speed data acquisition front end for real-time recorders, digital receivers and DSP systems.

Input Stage and A/D Converter

The 6826 features one or two Atmel AT84AS008 2 GHz, 10-bit A/D converters driven from single-ended transformer- or DC-coupled RF signals applied through front panel MMCX female connectors at -2 dBm full-scale into 50 ohms. Although the standard transformer-coupled input circuitry accepts signals to 1 GHz, higher frequency input options are also available.

An innovative dual-stage demultiplexer packs groups of eight data samples into 80-bit words for delivery to the FPGA at one eighth the sampling frequency ($f_s/8$). This advanced circuit features the Atmel AT84CS001 Demultiplexer that represents a significant improvement over previous technology.

Clocking, Gating and Triggering

The A/D converter sample clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz. This clock is accepted through a front panel MMCX connector with 50 ohm termination and distributed to both A/D converters (dual-channel version).

Synchronization and triggering circuitry supports synchronous data acquisition across multiple boards. Additional front panel MMCX connectors are provided for the

application of an $f_s/8$ clock to support multi-board synchronization.

Virtex-II Pro FPGA

The 6826 utilizes a Model XC2VP70 Xilinx Virtex-II Pro FPGA. The FPGA is equipped with 512 MB of DDR SDRAM (optionally expandable to 1 GB) and 16 MB of FLASH memory.

Several data packing modes allow formatting output data across multiple FPDP ports. The FPGA also acts as a controller for board functions such as gate/trigger. Optional LVDS I/O is available through either the VMEbus P2 connector or a second-slot front panel mezzanine.

FIFOs and FPDP Outputs

Following the FPGA, two or four 32-bit wide FIFO buffers with a depth of 32k words are useful as elastic memory to support hard disk latencies in recording applications.

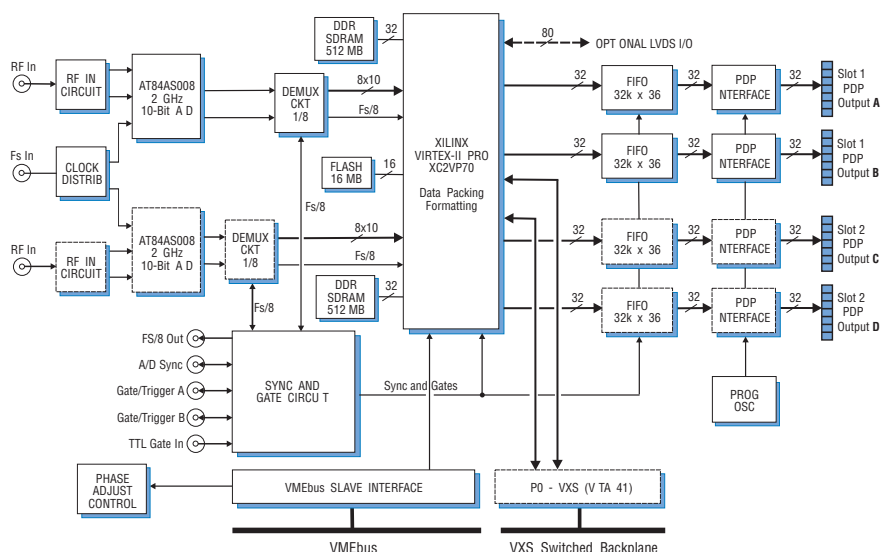
A total of four FPDP output ports are available, each supporting data transfers of up to 400 MB/sec. Two FPDP ports are attached to the 6826 front panel; optionally, two additional ports attach to a second slot front panel (not available in conduction-cooled units).

Optional VXS Interface

The 6826 provides two optional 4X full duplex VITA-41 links to the VXS P0 connector; each capable of peak rates to 1.25 GB/sec. These links support Gigabit fabrics such as Xilinx Aurora, Serial RapidIO and PCI Express.

Switchless VXS Card Cage

A five-slot card cage with full fabric support for three payload cards without the need for a switch card is available for developing and testing VXS cards. ➤



► Specifications

Front Panel Analog Signal Inputs

Quantity: 1 or 2

Input Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Input: -2 dBm into 50 ohms

Transformer 1 dB Passband: 50 MHz to 1 GHz

A/D Converters

Quantity: 1 or 2

Type: Atmel AT84AS008

Sampling Rate: 200 MHz to 2 GHz

Internal Clock: None

External Clock: 200 MHz to 2 GHz

Resolution: 10 bits

Bandwidth: 3.3 GHz at full power

Digital Demultiplexer Circuit

Quantity: 1 or 2

Overall Demux Ratio: 1:8

Initial Stage:

Type: Atmel AT84CS001

Demux Ratio: 1:4

Tunable Delay: -250 ps to +250 ps

Programmability: User-programmable

Output Resolution: 10 bits

Secondary Stage:

Type: Xilinx XC2VP4 FPGA

Demux Ratio: 1:2

Output Resolution: 10 bits

Clock Source: Front panel external clock

External Clock: Front panel female MMCX connector, sine wave, 0 to -2 dBm, AC coupled, 50 ohms impedance

A/D Sync Input/Output: Front panel female MMCX connector, low voltage PECL

Gate/Trigger Control: One or two front panel female MMCX connectors, low voltage PECL; one female MMCX connector, TTL

Field Programmable Gate Array

Quantity: 1

Type:

Option -070: Virtex-II Pro XC2VP70-6 FPGA I/O:

Option -121: Provides forty LVDS differential data I/O pairs, two clock I/O pairs and four control pairs from the FPGA to VMEbus P2 connector

Option -222: Adds two 68-pin connectors through a second-slot front panel; each provides twenty LVDS data I/O differential pairs, one LVDS clock I/O pair and two control I/O pairs

Memory

DDR SDRAM:

Quantity: Two banks

Size: 256 MB per bank, 512 MB total standard; 512 MB per bank, 1 GB total with option -340

Bus Width: 64 bits

Speed: 125 MHz; 250 MHz double data rate

FLASH:

Quantity: 1

Size: 16 MB

Bus Width: 16 bits

Front Panel Data Port (FPDP) Outputs

Quantity: 2 standard; 4 with option

-224 (additional ports located on second slot front panel)

Output Type: non-inverted configuration, FPDP I or FPDP II

Clock: Onboard programmable oscillator (up to 50 MHz)

FIFOs

Quantity: 2 standard, 4 with option -224

Size: 32,768 x 36

Speed: 133 MHz

VME Slave Interface

Type: Slave A16/D16, A16/D32, A24/D24 (A32/D32 programmable)

Control: Operating modes, gate/trigger, FIFO reset, data packing, FPDP I/II selection, status

Power

Default Configuration: 50 W (one A/D) to 60 W (dual A/D)

User FPGA designs will increase power consumption within the following ranges:

With XC2VP70 FPGA: from 50 W to 75 W typical

Environmental (Commercial version)

Pentek Ruggedization Level: L0

Cooling Method: Forced air

Operating Temp: 0 to 50° C

Storage Temp: -20 to 90° C

Relative Humidity: 0 to 95%, non-condensing

Environmental - Option -703

Pentek Ruggedization Level: L3

Cooling Method: Conduction cooling

Operating Temp: -40 to 70° C

Storage Temp: -50 to 100° C

Relative Humidity: 0 to 95%, non-condensing

Sine Vibration: 10 g, 20-2,000 Hz

Random Vibration:

0.1 g²/Hz, 20-2,000 Hz

Shock: 30 g, 11 ms

Environmental - Option -720

Relative Humidity: 0 to 100% non-condensing with conformal coating

Size: Standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 20.3 mm (0.8 in.) wide; Option -222 or -224: 40.6 mm (1.6 in.) wide

Weight: 1025 grams (2.26 lbs.)

Ordering Information

Model	Description
6826	Dual 2 GHz, 10-bit A/D with Virtex-II Pro FPGA - VME/VXS

Options:

-001	Single A/D Converter
-002	Dual A/D Converter
-070	XC2VP70 FPGA
-121	LVDS I/O through P2
-222	2nd Slot LVDS I/O
-224	2nd Slot FPDP I/O
-340	1 GB DDR SDRAM
-5xx	VXS Interface
-70x	Ruggedized & conduction-cooled versions



Features

- Thirty-two sigma-delta A/D channels
- 24-bit accuracy
- Differential inputs
- Programmable gain amplifiers
- FPDP (Front Panel Data Port) output
- Sampling rates from 1 kHz to 216 kHz
- 100 kHz anti-aliasing filters
- Internal or external sample clock
- Front panel sync bus synchronizes all channels on multiple boards
- Single slot 6U VMEbus board

Ordering Information

Model	Description
6802	32-Channel A/D with FPDP Output - VME
Option:	
-010	Differential 10 V p-p full-scale input voltage

General Information

Model 6802 is a high-performance 32-channel A/D converter board capable of sampling rates up to 216 kHz. As a single-slot VMEbus board, the Model 6802 includes both signal conditioning and clock generation circuitry. Output samples are delivered to a FPDP connector.

Signal Conditioning

The Model 6802 accepts 32 differential analog inputs with 16 channels on each of two front panel multipin connectors compatible with discrete wire termination.

Programmable-gain instrumentation amplifiers deliver each signal to a single-pole 100 kHz low pass anti-aliasing filter.

A/D Conversion

Sixteen monolithic, dual-channel sigma-delta A/Ds provide 32 channels of A/D conversion. Each A/D features 24-bit resolution at sampling rates ranging from 1 kHz to 216 kHz. These A/Ds provide excellent channel-to-channel matching and linear phase response, ideal for sonar and acoustic applications.

Sampling Control

The A/Ds utilize a high-speed system clock capable of 64x, 128x or 256x oversampling. This clock is sourced by an internal crystal oscillator or by an external clock supplied through a front panel DB9 connector. The internal oscillator can be replaced for custom sampling frequencies.

A programmable divider can be used to divide the internal or external system clock by a factor of 1, 2, 4, 8, 16, 32, 64 or 128.

Synchronization

The front panel sync input signal allows synchronization of up to eight 6802 boards. In addition, the front panel connector provides trigger signal I/O for data collection in the on-board FIFO memory.

FPDP Output

The number of active A/D channels can be selected from 1 to 32 in steps of 1. Data samples from all selected channels are then interleaved and stored in a 32-bit wide FIFO memory as either one 24-bit sample or two packed 16-bit samples.

The FIFO delivers samples from all selected channels to the FPDP output using 30 MHz PECL or 20 MHz TTL strobes.

Specifications

Input: differential, 2.4 V p-p full scale, DC coupled, each input 10 kohm to ground

Gain: 1, 10 or 100

Anti-aliasing filter: lowpass, $f_c = 100$ kHz

A/D converters: 24-bits, AKM AK5394,

SNR > 90 dB, THD < -100 dB FS

Sample Rate: 1 kHz to 216 kHz

System Clock: internal 12.800 MHz crystal oscillator, or external TTL clock via front panel connector (64 kHz to 13.824 MHz)

System Clock divider: divides internal or ext. clock by 1, 2, 4, 8, 16, 32, 64 or 128

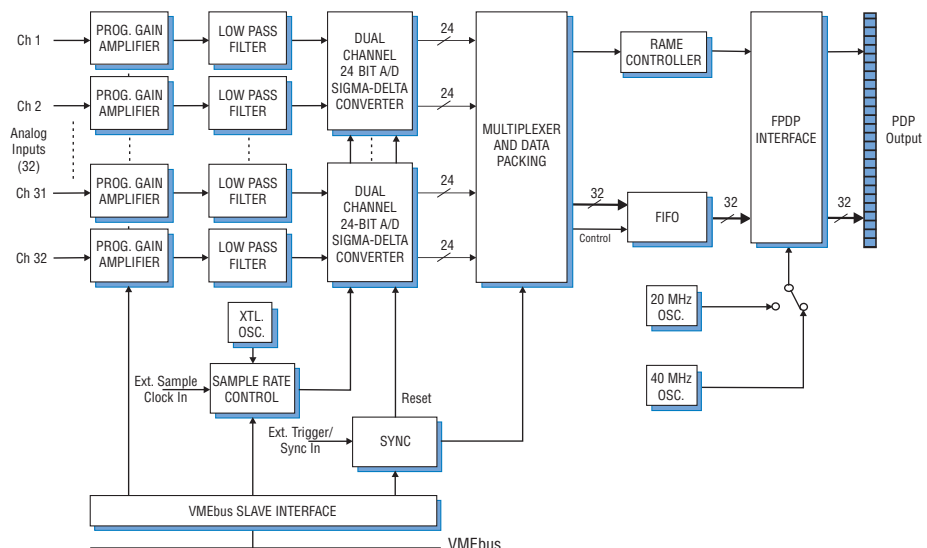
Output: FPDP, 32-bit, 30 MHz PECL strobe or 20 MHz TTL strobe

VME Interface

Type: slave A16 D16

Control: gain, channel selection, filters, operating modes, resets, data packing

Size: 6U board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide





Features

- VIM-2 module for VIM-compatible processor boards
- Provides two bidirectional FPDPs
- Data rates to 160 MB/sec

General Information

Model 6226 is a VIM-2 module which attaches directly to VIM-compatible processor boards. It makes two bidirectional FPDP ports available to the processors.

Two Model 6226's may be attached to a VIM-compatible processor board to provide four FPDP ports, one per processor. Alternatively, the Model 6226 may be combined with another VIM-2 module to provide additional I/O functions.

FPDP

FPDP (Front Panel Data Port) is an industry standard front panel ribbon interface, now defined by an ANSI/VITA specification, providing high speed data transfers between system peripherals, array processors and data acquisition devices. FPDP implements a 32-bit parallel communication link capable of delivering data at sustained rates of 160 MB/sec using standard flat ribbon cable.

Operation

The Model 6226 contains up to two identical sections, each providing a bidirectional FPDP port to its respective processor. A CPLD controller provides timing and handshaking to interface through the mezzanine connectors to the 32-bit mezzanine BI-FIFO ports of VIM processor boards. Each FPDP port can be software-configured for either input or output operation.

Options

The Model 6226 features one 80-pin FPDP connector on its front panel. This connector nests in the same slot as the VIM-compatible processor board. One of the following

options must be selected when purchasing (see drawings below for Options -002 through -004):

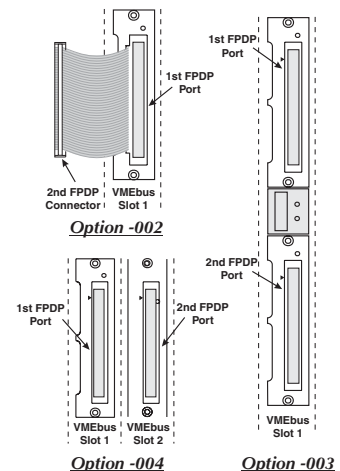
Option -001: Provides one FPDP port.

Option -002: Provides two FPDP ports in a single VIM-2 section. The first port is located on the front panel; the second port is accessible through a front panel ribbon cable terminated in a FPDP connector.

Option -003: Provides two FPDP ports in a single slot. The first port is located in the upper VIM-2 section; the second port is located in the lower section. No other VIM-2 module may be used with this configuration.

Option -004: Provides two FPDP ports in adjacent slots, allowing a second VIM-2 module to be connected. The second port is attached to an adjacent VME carrier panel which covers the entire second slot.

Two 6226's can be installed to provide up to four FPDP interfaces in a single slot (-002) or in two adjacent slots (-004).

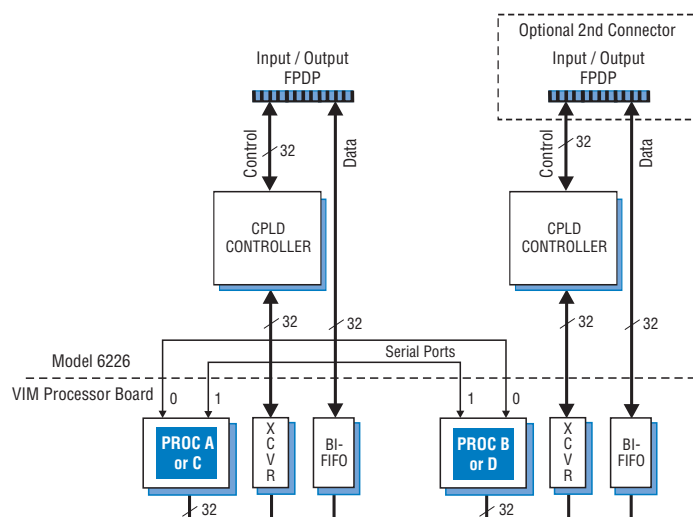


Ordering Information

Model	Description
6226	FPDP Adapter - VIM-2

Options:

-001	One FPDP
-002	Dual FPDP, plug & cable
-003	Dual FPDP, in-line
-004	Dual FPDP, two slots





Features

- Two low distortion 105 MHz 14-bit A/D converters
- Internal or external A/D sample clock to 105 MHz
- Advanced Virtex-II FPGA for signal preprocessing
- Front panel sync bus
- ASIC and FPGA wideband downconverter options

Ordering Information

Model	Description
6236	14-bit A/D with FPGA and Optional Downconverters - VIM-2

Options:

-102	Front panel FPGA I/O (additional slot)
-212	Two ASIC Graychip GC1012B Wideband Digital Downconverters
-421	GateFlow Wideband 2-Ch Digital DDC Core in FPGA
-300	Xilinx XC2V3000 FPGA replaces XC2V1000

General Information

Model 6236 is a dual 14-bit A/D VIM-2 module. It attaches directly to VIM-compatible baseboards and includes a Virtex-II FPGA (Field Programmable Gate Array) as well as optionally available wideband digital receivers.

Front End

The Model 6236 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors.

Each of the two inputs is transformer coupled and digitized by an Analog Devices AD6645-105 14-bit A/D converter. The AD6645 is capable of operating at sample rates from 30 MHz to 105 MHz.

The A/D converter clock can be driven from an internal crystal oscillator or from an external sample clock supplied through a front panel SMA connector or front panel sync bus.

FPGA

The A/D outputs are delivered to a Xilinx Virtex-II FPGA (Model XC2V1000 standard; XC2V3000 optional) which is factory configured to perform various modes of data packing, formatting and channel selection. The A/D outputs are connected directly to the FPGA so that wideband A/D data can be delivered directly to the DSP board.

Optionally available design kits allow the FPGA to be configured by the user for implementation of custom preprocessing functions such as convolution, framing, pattern recognition and decompression.

Optional Digital Downconverters

The 6236 offers two different wideband digital downconverter options, each featuring a decimation range from 2 to 64.

Option -212 adds two bypassable Graychip GC1012B downconverter ASICs with 40 MHz maximum bandwidth for a 100 MHz sample clock, 75 dB stopband attenuation, 12-bit input and 16-bit output.

Option -421 adds a dual-channel GateFlow Downconverter Installed Core within the FPGA with 42 MHz maximum bandwidth for a 105 MHz sample clock, 100 dB stopband attenuation, 14-bit input, 24-bit output and programmable filter coefficients.

Synchronization

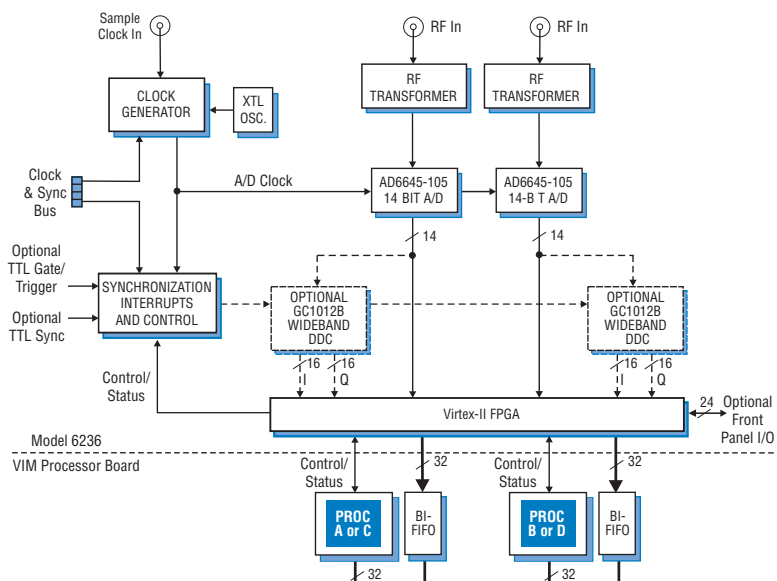
The front panel clock and sync bus allow one 6236 to act as a master driving the sample clock out to a front panel cable bus using LVDS differential signaling. Multiple slaves can then be clocked synchronously with the master.

Front Panel I/O

An optional front panel connector provides digital input and output for the FPGA. These lines are available for triggering, synchronizing, or framing signals. They are also useful during FPGA algorithm development for timing and signal probing.

VIM Processor Interface

The FPGA outputs are connected directly through the VIM mezzanine interface to the 32-bit synchronous BI-FIFO on the VIM processor board where it is buffered for efficient block transfers into the DSP.





Features

- Supports high-performance custom signal processing
- One or two FPDP (Front Panel Data Port) interfaces
- Xilinx Virtex-II Series FPGAs
- Two gate densities available: 1000K & 3000K
- On-board auxiliary SRAM
- GateFlow FPGA Design Kit
- Factory-installed cores available

General Information

Model 6250 is a Configurable Logic FPGA VIM-2 module with FPDP I/O. It features up to two FPDP (Front Panel Data Port) interfaces, and two Xilinx Virtex II FPGAs (Field Programmable Gate Arrays).

The Model 6250 supports custom, high-performance signal processing and computing functions for any VIM-compatible processor board.

FPGA Devices

The Model 6250 may be equipped with two FPGAs from either Xilinx Virtex-II family: Model XC2V1000 (standard), or XC2V3000 (Option -300).

Each FPGA interfaces directly to all three sections of the associated VIM interface: both serial ports, the 32-bit BI-FIFO parallel port and the control/status port. The BI-FIFO buffers on the processor board allow the processors to move blocks of data efficiently to and from each FPGA.

The two FPGAs are interconnected with up to 68 (XC2V3000) programmable user I/O lines to support data and control passing between the two devices. An optional connector is available for FPGA front panel I/O (Option -102).

SRAM

Each FPGA is equipped with two 256k x 16 SRAMs. Each SRAM is connected to the FPGA with separate address and data buses so they can be used independently. The SRAMs can be used for storing data without consuming internal FPGA logic cells to implement RAM.

FPDP Interfaces

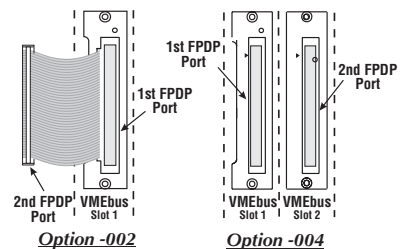
One FPDP interface is provided as standard with an additional interface available in two different optional configurations: single-slot, with the second connector accessible through a front panel ribbon cable (Option -002), or two slots with the second connector in an adjacent slot (Option -004).

FPGA Programming

An optional FPGA design kit to be used in conjunction with the Xilinx Foundation development tool suite is provided. It includes VHDL source files for the VIM interface and control registers for the clock functions. Templates for implementing custom signal processing blocks are included with detailed instructions. FPGA code may be downloaded from the processor node or permanently stored in non-volatile memory.

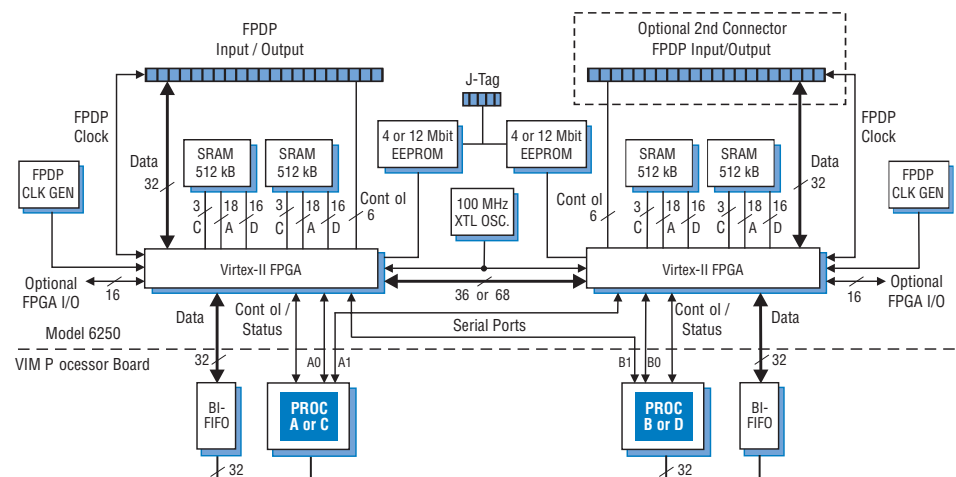
Numerous third-party sources for IP signal processing core libraries compatible with the Virtex-II support a wide range of popular algorithms and functions. These include FFTs, FIR filters, compression and decompression algorithms, software radio blocks, decryption, telemetry functions, decoders, encoders, and convolution.

In addition, the GateFlow FPGA Design Kit is optionally available from Pentek.



Ordering Information

Model	Description
6250	Configurable Logic FPGA with FPDP I/O - VIM-2
Options:	
-002	Dual FPDP, plug and cable
-004	Dual FPDP, two slots
-102	Front panel FPGA I/O (additional slot)
-300	Xilinx XC2V3000 FPGAs
-404	4k-point quad FFT core installed





Features

- Supports high-performance custom signal processing
- One or two FPDP or LVDS I/O front panel interfaces
- Xilinx Virtex-II Pro FPGAs
- FPGA configuration package includes VHDL source code and design examples
- FPGA configuration code can be downloaded from processor nodes or stored in non-volatile EEPROM
- On-board auxiliary SDRAM and FLASH memory
- Factory-installed cores available

General Information

The Model 6251 is a Configurable Logic FPGA VIM-2 (Velocity Interface Mezzanine) module with optional FPDP (Front Panel Data Port) or LVDS I/O. It features one or two front panel interfaces, and two Xilinx Virtex-II Pro FPGAs.

As a VIM-2 module, Model 6251 connects to one of the two VIM-2 sites on a VIM base-board, leaving the other site available for a second VIM-2 module of any type.

FPGA Devices

The Model 6251 is equipped with two of several FPGA devices in the Xilinx Virtex-II Pro family including Models XC2VP20 and XC2VP50 (selectable by option number). Contact factory for alternate sizes.

Each FPGA interfaces directly to all three sections of the associated VIM interface: the serial ports, 32-bit BI-FIFO parallel port and control/status port. The VIM BI-FIFO buffers on the processor board allow the processors to move blocks of data efficiently to and from each FPGA.

The two FPGAs are interconnected with 84 programmable user I/O lines to support data, clocking and control passing between the two devices.

Memory

Each FPGA is equipped with a 16M x 32 (64 MB) SDRAM connected with separate address and data buses so it can be used independently. These SDRAMs are useful for storing data without consuming internal FPGA logic cells. In addition, 16 MB of FLASH memory is attached to each FPGA, for a total of 32 MB.

Front Panel I/O Interfaces

The 6251 offers several configurations of front panel FPGA I/O. First, an optional multipin front panel connector provides LVDS I/O in the first slot (option -007), or in an adjacent slot (option -122). These options can be combined to obtain LVDS I/O from both of the on-board FPGAs.

An additional I/O solution is the optional FPDP interface in the first slot (option -008), or an adjacent slot (option -014). These options can be combined to obtain FPDP I/O from both on-board FPGAs. Alternatively, option -008 can be combined with option -122 to achieve both FPDP and LVDS I/O simultaneously.

These numerous 6251 front panel possibilities are achieved by the use of unique Pentek "personality modules". This flexible design makes it possible for a user to create custom I/O modules.

FPGA Programming

Pentek's optional GateFlow Design Kit allows the FPGAs to be configured by the user for implementation of custom preprocessing functions such as FFTs, FIR filters, compression and decompression algorithms, software radio blocks, decryption, decoders and encoders, and convolution.

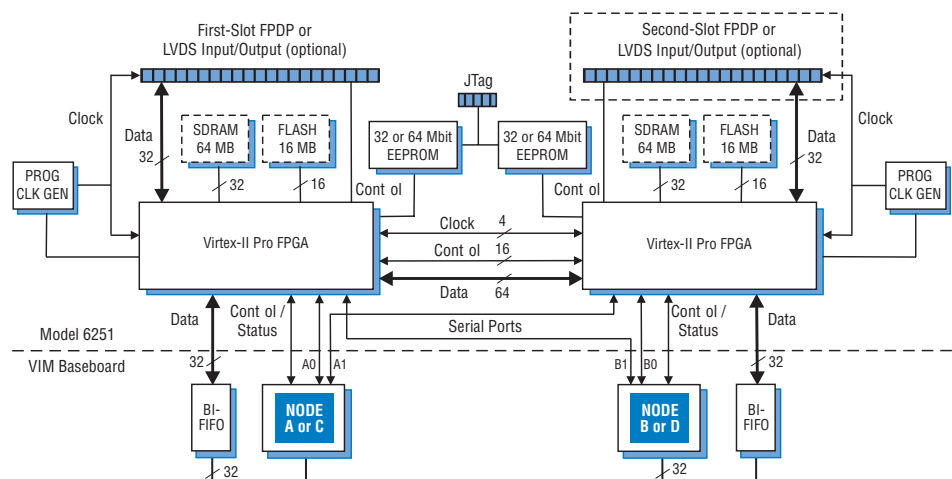
The GateFlow FPGA Design Kit is used in conjunction with the Xilinx Foundation development tool suite, and includes VHDL source files for the VIM interface and control registers for clock functions. Templates for implementing custom signal processing blocks are also included. FPGA code may be loaded from the processor or permanently stored in non-volatile memory.

Ordering Information

Model	Description
6251	Configurable Logic & I/O with Virtex-II Pro FPGA - VIM-2

Options:

-007	First-slot LVDS I/O
-008	First-slot FPDP I/O
-014	Second-slot FPDP I/O
-020	XC2VP20 FPGAs
-050	XC2VP50 FPGAs
-122	Second-slot LVDS I/O
-340	64 MB SDRAM and 16 MB FLASH per FPGA





PENTEK PROCESSORS

PROCESSORS

MODEL	DESCRIPTION
4207	MPC 8641 PowerPC I/O Processor with Virtex-4 FPGA - VME/VXS
4205	PMC/VIM Carrier MPC7457 PowerPC Processor - VME
4293	Octal TMS320C6203 Processor PMC/VIM - VME
9220	Triple PMC Expansion Board - VME
	Customer Information

[Click Here for the PRODUCT SELECTOR](#)

Last updated: November 2010



Features

- Freescale MPC8641 single or dual core PowerPC processor to 1.5 GHz
- Xilinx Virtex-4 FX Series FPGA
- Hosts two PMC or XMC modules
- On-board dual gigabit Ethernet interfaces
- Optional on-board 4-Gbit dual optical Fibre Channel controller
- Optional dual optical gigabit serial / Fibre Channel interface
- Up to 3 GB DDR2 SDRAM
- Two 64-bit PCI-X buses
- VME64x master/slave interface
- Optional VXS interface
- **Ruggedized and conduction-cooled versions**

General Information

The Pentek Model 4207 PowerPC™ VME/VXS I/O Processor board targets embedded applications that require high performance I/O and processing. With two PMC/XMC module sites, the 4207 offers powerful one-slot solutions with nearly unlimited high-speed connectivity.

Uniquely Designed for Connectivity

The 4207 supports numerous interfaces including VME64x, Gigabit Ethernet, RS-232 and dual 4 Gbit Fibre Channel. A unique crossbar switch architecture connects the XMC module sites, optical and VXS connectors, fibre channel interface, FPGA, and processor to high-speed gigabit serial data paths. All interfaces can be included without exceeding one VMEbus slot. Some processing-intensive applications may require two slots for optimized convection cooling.

MPC8641 AltiVec Processor

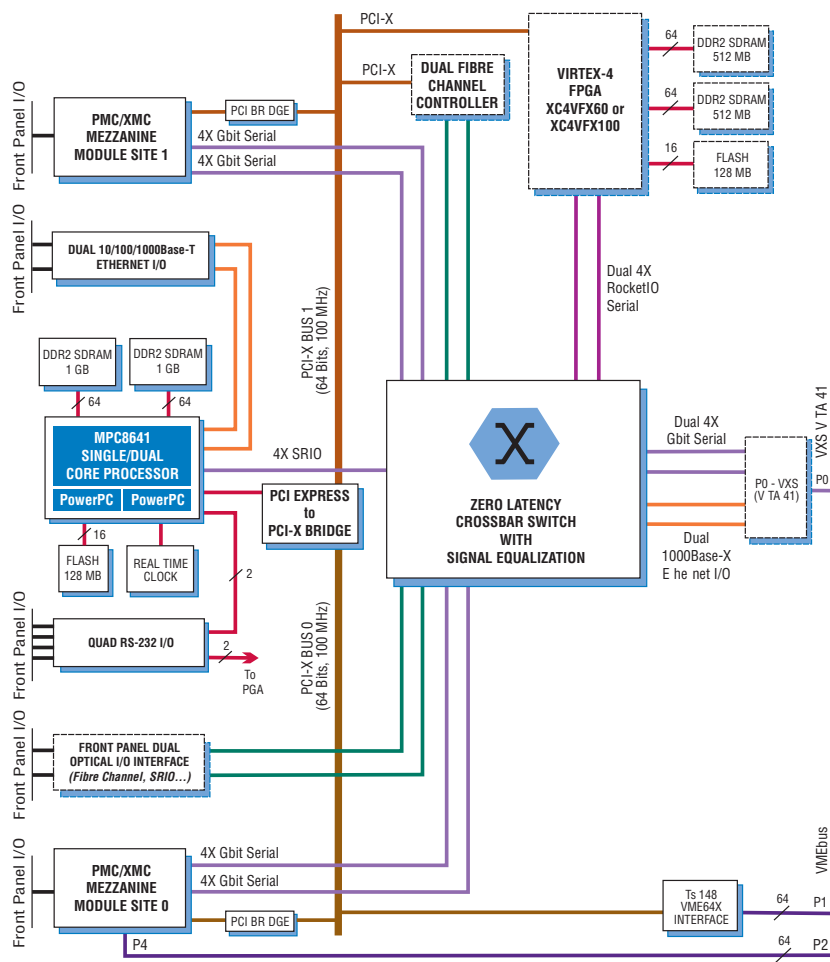
The Freescale MPC8641 utilizes the AltiVec™ engine to perform parallel processing of multiple data elements (SIMD) with 128-bit operations. The AltiVec processor

executes both fixed- and floating-point instructions. It is available with either a single or dual e600 PowerPC core with maximum clock frequency of 1.5 GHz. Built-in gigabit serial data ports provide 4X Serial RapidIO.

Zero Latency Crossbar Switch

The 4207 features a zero-latency fabric-transparent crossbar switch that bridges various board interfaces and resources via gigabit serial data paths. Programmable signal input equalization and output pre-emphasis settings enable optimization for each application.

Gigabit serial paths include links to the processor that can be used for 4X Serial RapidIO. Other gigabit paths are not restricted to any protocol, and include two 4X links to each XMC module site, two 4X links (or four 2X links) to the FPGA RocketIO ports, and another pair of 4X links to the optional P0-VXS connector. The switch also provides high-speed connectivity to the optional Fibre Channel controller and front panel optical gigabit serial interface. ➤



Support Software

The Model 4207 is supported by world-class software for initialization, control and optimization.

Pentek **VxWorks BSPs** provide software developers with a complete library of hardware initialization, control and application functions. Used in conjunction with Wind River's **Workbench** software development environment, it speeds application development.

Pentek **Linux BSPs and Drivers** provide software developers with a complete open-source library of hardware initialization, control and application functions to be used in a real-time Linux operating environment.

Pentek **GateFlow® Design Kits** allow the onboard FPGA to be configured by the user for implementation of custom pre-processing functions. The kit is used in conjunction with the Xilinx ISE *Foundation™* design tools.

Verari Systems' **VSI/Pro** is an implementation of VSIPL scientific and engineering functions optimized for the PowerPC.



Ordering Information

Model	Description
4207	MPC8641 PowerPC I/O Processor with Virtex-4 FPGA - VME/VXS
Options:	
-001	Front Panel Optical Connectors/Transceivers
-006	Dual Fibre Channel interface, 4 Gbit/sec
-013	Single core 1.33 GHz MPC8641 w/1 GB DDR2
-023	Dual core 1.33 GHz MPC8641D w/1 GB DDR2
-123	Dual core 1.33 GHz MPC8641D w/2 GB DDR2
-061	XC4VFX60-11 FPGA
-101	XC4VFX100-11 FPGA
-360	1 GB FPGA DDR2 SDRAM + 128 MB FLASH
-5xx	VXS interface
-70x	Ruggedized & conduction-cooled versions

► PMC/XMC Mezzanine Sites

Model 4207 includes two 64-bit PMC module sites which accept industry-standard modules up to 133 MHz for a wide variety of functions. The PMC modules are accessible from the MPC8641 processor and the VMEbus. A PCI bridge at each PMC site allows operation of slower 33 or 66 MHz modules while running the attached PCI-X bus at a higher speed.

The 4207 PMC sites are also equipped to accept XMC (switched-fabric PMC) modules. Gigabit switched-fabric connectors are optionally provided to support two 4X full-duplex serial ports per XMC site. Each port allows high-speed data transfer to the crossbar switch using gigabit fabrics such as Xilinx Aurora or Serial RapidIO.

FPGA Devices

The 4207 optionally includes a Xilinx Virtex-4 FX Series FPGA, the XC4VFX60 or XC4VFX100. Two 4X RocketIO ports provide a high-speed serial data path to and from the FPGA. These ports can also be configured as four 2X paths.

Unused FPGA resources are available for the user to implement custom signal-processing configurations and algorithms using Pentek's GateFlow® FPGA Design Kit and the high-performance IP Core Library.

Memory

The 4207 provides a wealth of memory resources with up to 3 Gigabytes of DDR2 SDRAM and 256 MB FLASH.

The MPC8641 PowerPC is equipped with two 64-bit banks of DDR2 SDRAM at 512 MB or 1 GB each, for up to 2 GB program and data memory. A nonvolatile 128 MB FLASH memory is also provided for initialization, self-test and boot code. 1 MB on-chip L2 cache is available per processor core.

The Virtex-4 FX Series FPGA is optionally equipped with another two 64-bit banks of DDR2 SDRAM at 512 MB each, and 128 MB FLASH memory.

Two PCI-X Buses

The Model 4207 architecture includes two 64-bit PCI-X buses. PCI-X Bus 0 provides access to the VMEbus and its associated PMC/XMC mezzanine site. PCI-X Bus 1 provides access to its associated PMC/XMC mezzanine site, and the optional dual Fibre Channel interfaces.

Dual Fibre Channel Interface

The 4207 features an optional dual Fibre Channel controller with optical front panel interface for high-speed data transfer to and from Fibre Channel storage devices. When installed, both optical interfaces are located on the 4207 front panel, along with the dual 10/100/1000Base-T Ethernet and the quad RS-232 interfaces. This allows Fibre Channel data transfer without sacrificing a PMC/XMC site, thus maintaining a single VMEbus slot.

VXS Interface

The 4207 provides two optional 4X full-duplex VITA-41 VXS links to the P0-VXS connector, each capable of peak rates up to 1.25 GB/sec. Each link is attached to the crossbar switch, and compatible with gigabit fabrics such as Xilinx Aurora and Serial RapidIO. The P0-VXS connector also features a dual 1000Base-X Ethernet interface per the VITA 41.6 draft standard.

Specifications

Processor Resources

Processor: Freescale MPC8641 (Single Core) or MPC8641D (Dual Core)

Processor clock: 1.33 GHz (-013 or -023)
Contact factory for options from 1 - 1.5 GHz

Level 2 cache: 1 MB for MPC8641, 2MB for MPC8641D

DDR2 SDRAM: 1 GB or 2 GB (optional, one or two 1 GB banks, each 64 bits wide)

FLASH: 128MB, 16 bits wide

Node Control: Built into MPC8641

Mezzanines

Two PMC/XMC sites

Optional FPGA

Type: Xilinx Virtex-4 Series (-11 speed) XC4VFX60 (-061) or FX100 (-101)

DDR2 SDRAM: 1 GB (optional, two 512 MB banks, each 64 bits wide)

FLASH: 128 MB, 16 bits wide (optional)

PCI-X Bus #0

Width: 64 bits, **Speed:** 100 MHz

PCI-X Bus #1

Width: 64 bits, **Speed:** 100 MHz

Global Resources

VME64x: Tundra Tsi148 master/slave, slot 1 controller, D64, A32

Serial I/O: Four RS232 front panel ports

Ethernet: Two 10/100/1000Base-T front panel ports, two 1000Base-X ports on rear P0-VXS connector

Optional Fibre Channel Controller:

Dual Optical, 4 Gbit (Option -006)

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide



Features

- Freescale 1.267 GHz MPC7457 G4 PowerPC processor
- Xilinx Virtex-II FPGAs
- Selectable FPGA data flow architecture
- Hosts one PMC plus one VIM-2 module, two VIM-2 modules, or one VIM-4 module
- Optional onboard Fibre Channel interface
- Optional onboard Gigabit Ethernet interface
- 2 MB L3 cache
- Up to 1 GB SDRAM
- Two 64-bit PCI buses
- VME64 master/slave interface

General Information

Model 4205 Single PowerPC VIM/PMC Carrier board targets embedded applications requiring high performance I/O and processing. The board maintains the lower cost of a single-processor baseboard and features a Freescale MPC7457 and two Xilinx Virtex-II FPGAs. The Model 4205 offers one-slot solutions with two VIM-2 modules, one VIM-4 module, or one VIM-2 and one PMC module.

In addition to its mezzanine I/O capabilities, the 4205 supports numerous interfaces including VME64, Ethernet, RS-232 and, optionally, Fibre Channel and Gigabit Ethernet.

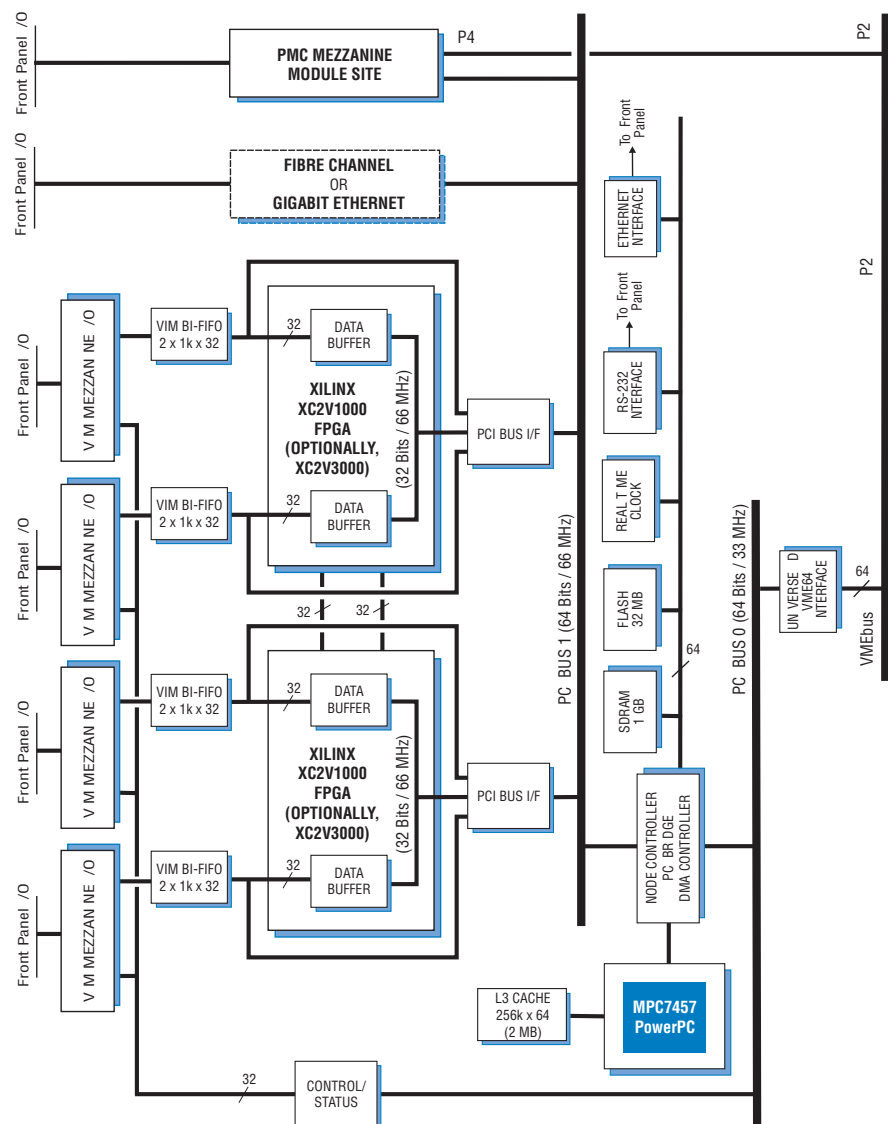
All interfaces can be included without exceeding the one-slot configuration.

MPC7457 AltiVec Processor

The Freescale MPC7457 utilizes the AltiVec engine to perform parallel processing of multiple data elements (SIMD) with 128-bit operations. The AltiVec processor executes both fixed- and floating-point instructions, augmenting the separate integer and floating point units also on the chip.

FPGA Devices

The 4205 also includes two on-board Xilinx Virtex-II XC2V1000 FPGAs that provide a high-speed synchronous bidirectional streaming data interface for each VIM mezzanine connector. This allows buffering of 32-bit parallel data transfers between VIM mezzanine modules, the MPC7457 and global resources. An interconnect path is provided between the FPGAs for additional flexibility. To optimize ➤



Support Software

Pentek **VxWorks BSPs** provide software developers with a complete library of hardware initialization, control and application functions. Used in conjunction with Wind River's **Workbench** software development environment, it speeds application development.

VSI/Pro from Verari Systems Software is an implementation of VSIPL scientific and engineering functions optimized for the PowerPC.

Pentek **ReadyFlow** Board Support Libraries provide support for VIM and PMC mezzanines. They consist of C-callable libraries for board-specific functions.

In addition, ReadyFlow for PowerPC-based processor boards includes a complete distribution of **eCos**, an open source, royalty-free, real-time operating system intended for embedded applications. eCos-based applications can be developed with the included GNU development tools: the GCC C-language compiler, GDB debugger and Insight GUI interface for GDB.



Ordering Information

Model	Description
4205	PMC/VIM Carrier MPC7457 PowerPC Processor - VME
Options:	
-006	Front panel Fibre Channel interface, 1 or 2 Gbit/sec
-007	Front panel Gigabit Ethernet interface (1000Base-T)
-057	1 GHz MPC7457
-058	1.267 GHz MPC7457
-300	XC2V3000 FPGAs replace XC2V1000
-322	16 kB VIM BI-FIFO
-340	1 GB SDRAM

► performance for specific applications, different data flow and control architectures for the FPGAs can be selected from a menu of built-in configurations. For example, a dual-port RAM structure is available for applications that require random access I/O.

A large percentage of the 4205 FPGA resources is available to users to implement custom signal processing configurations and algorithms. Available resources can be increased with the optional XC2V3000 FPGAs.

VIM Mezzanine

The 4205 is equipped with four VIM (Velocity Interface Mezzanine) connectors. Each of these connectors is attached to one of the two on-board Xilinx Virtex-II Series FPGAs.

The VIM architecture allows simultaneous I/O data transfer from all four VIM mezzanine interfaces with no contention for shared resources. Data can then be transferred to global resources, front or rear panel I/O, or between VIM modules. Control and status registers on the VIM modules can be read and written to as memory mapped resources of the MPC7457 or the VMEbus.

PMC Mezzanine Site

In addition to accommodating Pentek's broad range of VIM I/O peripherals, Model 4205 incorporates a 64-bit 66 MHz PCI Mezzanine Card (PMC) module site which accepts industry-standard modules for a wide variety of interface and communication functions. The PMC module is accessible from the MPC7457 processor and the VMEbus.

Memory

The MPC7457 is equipped with 256 kB on-chip L2 cache. This is supplemented by 2 MB of L3 cache. A 512 MB SDRAM, which may be optionally increased to 1 GB, is provided for program and data memory, along with a nonvolatile 32 MB FLASH memory for initialization, self-test and boot code.

Dual PCI Buses

The Model 4205 architecture includes dual 64-bit PCI buses. PCI Bus 0 provides access to the VMEbus and optional RACEway interface, as well as VIM mezzanine address and data control.

PCI Bus 1 provides a high-speed path to both VIM and PMC mezzanine sites, as well as optional front panel I/O such as Fibre Channel, Gigabit Ethernet or Serial FPDP.

Optional Fibre Channel Interface

The 4205 features an optional front panel copper Fibre Channel interface for high speed data transfer to and from Fibre Channel storage devices. When installed, this interface is located on the 4205 front panel along with 10/100Base-T Ethernet and RS232. This allows Fibre Channel data transfer without taking up a VIM or PMC site, maintaining a single VMEbus slot.

Optional Gigabit Ethernet Interface

The 4205 features an optional Gigabit Ethernet interface for high speed communications with other devices. This interface is also located on the front panel along with 10/100Base-T Ethernet and RS232. It provides a bidirectional port capable of 10, 100 or 1000Base-T data transfer speeds. This interface does not take up a VIM or PMC site, thus maintaining a single VMEbus slot.

Specifications

Processor Resources

Processor: Freescale MPC7457

Processor clock: 1 GHz, 1.267 GHz

Level 3 cache: 256k x 64 (2 MB)

Node Control: Marvell GT-64260

Mezzanines

Two VIM-2 sites, one PMC site

FPGAs

Xilinx XC2V1000 std; XC2V3000 optional

PCI Bus #0

Width: 64 bits

Speed: 33 MHz

PCI Bus #1

Width: 64 bits

Speed: 33/66 MHz

Global Resources

VME64: Tundra Universe IID master / slave, slot 1 controller, D64, A32

Serial I/O: RS-232 front panel port

Ethernet: 10/100Base-T front panel port

SDRAM: 512 MB, 1 GB (optional)

FLASH: 8M x 32 (32 MB)

Fibre Channel: Copper, 2 Gbit (optional)

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide



General Information

Designed for applications requiring extremely high-speed signal processing and data transfers, the Model 4293 features eight Texas Instruments TMS320C6203 DSPs operating at 300 MHz and delivering a combined peak processing capability of 19,200 MIPS.

TMS320C6203 DSP

As a member of the C6000 family, the C6203 utilizes TI's new 0.15 micron process which delivers 896 kB of on-chip SRAM, 512 kB for data and 384 kB for program, eliminating the need for external memory access in many applications.

The VLIW engine executes up to eight instructions in a single 300 MHz clock cycle, delivering up to 2400 MIPS. The powerful DMA controller transfers data to peripherals over dual 32-bit external data buses at rates

as high as 600 MB/sec. Three serial ports easily support popular telecom interfaces.

Overall Circuit Description

Four identical dual processor nodes contain interface and memory resources ideally matching the I/O capabilities of the C6203 to high-performance system components.

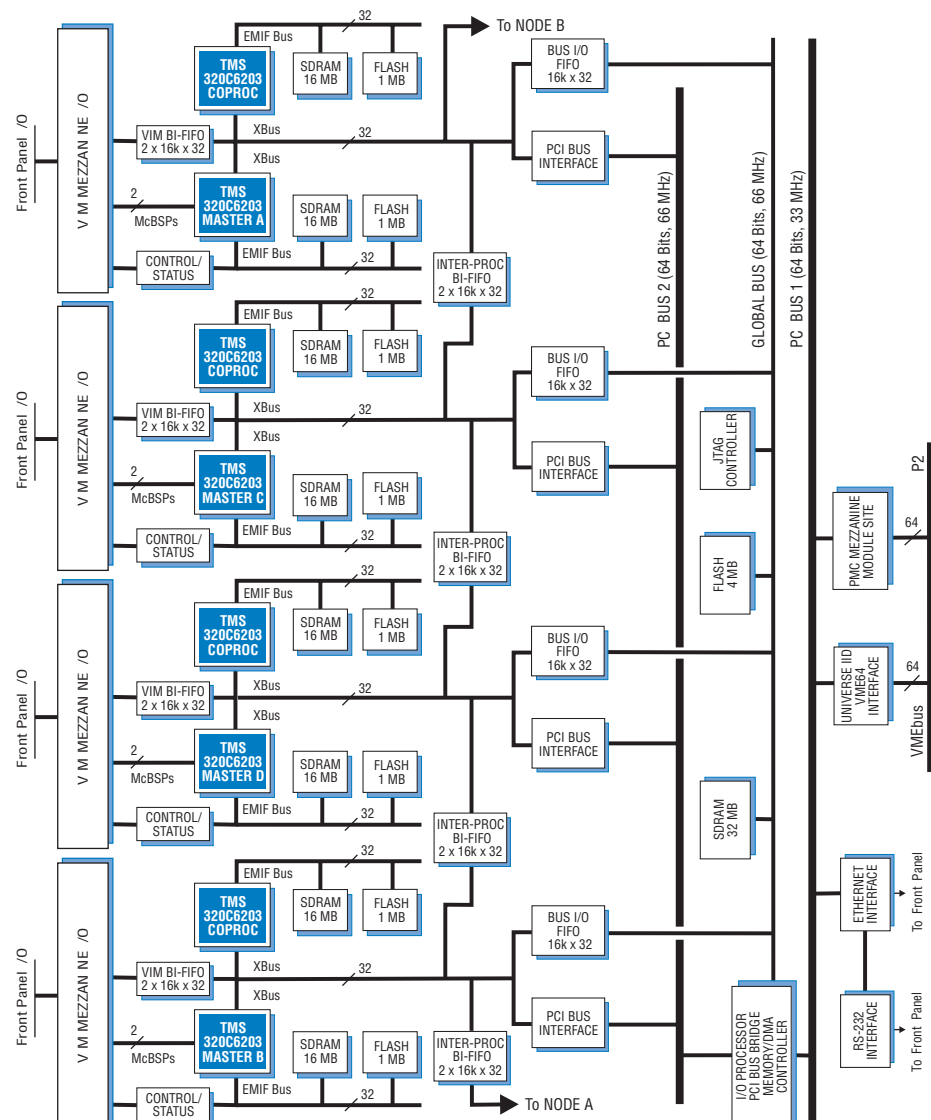
Each node contains two C6203 devices, a master and a coprocessor, both equipped with local SDRAM and FLASH memory.

The master controls the VIM high-speed mezzanine interface, interprocessor links, a dedicated bus I/O channel, and connections to powerful shared board resources. It moves data in and out of the internal data and program memory resources of the coprocessor and controls its execution.

The coprocessor and its private external SDRAM can be used very effectively to off-load compute-intensive signal processing ➤

Features

- Eight 300 MHz TMS320C6203 DSPs
- 19,200 MIPS peak processing power
- High-performance PMC and VIM mezzanine module sites
- Four 300 MB/sec VIM mezzanine I/O BI-FIFOs
- Four 300 MB/sec interprocessor BI-FIFOs
- Four 300 MB/sec Bus I/O FIFOs
- Eight 8 MB or 16 MB SDRAMs with 600 MB/sec transfer rates
- 32 MB of shared global SDRAM
- VME64 master/slave interface



Support Software

Pentek's **SwiftNet** supports a network of distributed VMEbus systems and allows the developer to run development tools on the host, while maintaining remote access to the VMEbus system.

Pentek's **ReadyFlow** Board Support Libraries reduce development time by providing C-language callable functions for hardware initialization, control and operation of board resources.

TI's **Code Composer Studio** provides a comprehensive set of tools for software development including an optimizing C Compiler, an interactive debugger, the DSP/BIOS operating system and an assortment of profiling and optimizing tools.



Ordering Information

Model	Description
4293	Octal C6203 Processor PMC/VIM - VME

Options:

-320	16 kB VIM and IP BI-FIFO, 16 kB Bus I/O FIFO
-340	16 MB local SDRAM (8 MB std.)

* Contact Pentek for PMC compatibility

► tasks from the master. When each task is completed, the coprocessor can notify the master efficiently through an interrupt.

VIM Mezzanine

Each dual processor node is equipped with its own VIM connector, providing three types of interfaces.

A high-speed synchronous bidirectional FIFO (BI-FIFO) buffers 32-bit parallel data transfers between the mezzanine and the master C6203's expansion bus (Xbus) at rates up to 300 MB/sec. Two of the master C6203's 50 Mbit/sec synchronous serial ports are also brought to the VIM mezzanine connector. The third serial port joins all eight processors for an additional link. The External Memory Interface (EMIF) bus of the master C6203 provides memory-mapped control and status functions to the mezzanine circuitry.

Local Memory

Two types of local memory resources are provided for each C6203: up to a 16 MB SDRAM and a nonvolatile 1 MB FLASH memory for initialization, self-test and boot code.

Interprocessor BI-FIFOs

Because the C6203 includes no inter-processor communication links, the Model 4293 features four bidirectional FIFOs joining the EXP buses of each processor node in a ring structure. Each master C6203 can send and receive interprocessor data blocks at 300 MB/sec without having to arbitrate for a shared resource.

Bus I/O FIFOs

By using private Bus I/O FIFOs, each master processor can transfer blocks of data from global resources including RACEway, global SDRAM, VMEbus and the PMC site. These FIFOs eliminate wait cycles by effectively decoupling the C6203's from these resources and allowing 300 MB/sec block transfers to the nodes.

PCI Master Interface

Each master C6203 can master the PCI bus for read/write access to RACEway, VMEbus, global SDRAM and the PMC site.

Global SDRAM

Serving as a convenient shared resource for staging data, the 32 MB global SDRAM is accessible from all four master C6203's, the VMEbus, RACEway and the PMC site.

Ethernet/RS-232 Interface

Front panel 100Base-T and RS-232 interfaces provide a gateway for debugging during development, and data transfers at run time.

PMC Site

The PCI Mezzanine Card (PMC) module site accepts most industry-standard modules for a wide variety of interface and communication functions. The PMC module is accessible from all four master C6203's and from the VMEbus.

Peripheral I/O

Model 4293 may be equipped with two VIM-2 modules, either identical or providing different functions; one VIM-4 module; or one VIM-2 module in the upper position and one PMC module in the lower position.

VME64 Interface

All four master C6203's can master the VMEbus using the industry standard Universe II VME64 interface chip. As a VMEbus slave, the Model 4293 presents the global SDRAM, the four Bus I/O BI-FIFOs, and the PMC site as memory mapped resources.

Specifications

Processor Node Resources: 4 total

Processors: two Texas Instruments

TMS320C6203's per node

Processor Clock: 300 MHz

SDRAM: Dual 4M x 32

FLASH: Dual 1M x 8

Mezzanine: VIM site

Mezzanine BI-FIFO: 2 x 1k x 32;

2 x 16k x 32 optional

Interprocessor BI-FIFO: 2 x 1k x 32;

2 x 16k x 32 optional

Bus I/O FIFO: 1k x 32; 16k x 32 optional

Shared Global Resources:

Global SDRAM: 4M x 64

FLASH: 4M x 8

VME64: Tundra Universe II master/slave, slot 1 controller

PMC Module Site: 64 bit, 33 MHz, 5 V

Front Panel Interfaces: 100Base-T, RS-232

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide



Shown with Model 4205 PowerPC I/O Processor featuring built-in Fibre Channel. Attached Pentek PMC and VIM I/O modules include 48 DDC channels, 6 A/D channels, 4 D/A channels and 4 DUC channels.

Features

- Adds three PMC sites to Pentek baseboards
- Allows simultaneous mounting of PMC and VIM modules on Pentek baseboards
- Does not use any baseboard power
- LVDS connectivity from PMC P4 to VME P2
- Optional connectivity from PMC P4 connector to VME P2 rows Z and D
- Optional P4 connectivity between PMC modules

Ordering Information

Model	Description
9220	Triple PMC Expansion Board - VME

Options:

-151	P4 connectivity from PMC Site 2 to P2 Rows Z and D
-152	P4 connectivity between PMC Sites 1 and 2

General Information

Model 9220 provides additional PCI Mezzanine Card (PMC) sites for compatible Pentek baseboards including Models 4205 and 4295. It extends the baseboard PMC connector into a second VMEbus slot where up to three PMC modules can be mounted. This additional PMC support does not interfere with baseboard VIM mezzanine sites, so that up to three PMC modules and two VIM modules can be mounted on a single baseboard simultaneously.

PMC Mezzanine Sites

Model 9220 incorporates three 64-bit 66 MHz PMC module sites, each accepting industry-standard modules for a wide variety of interface and communication functions. The 9220 accommodates both 3.3V and 5V PMC modules without drawing power from the attached baseboard.

Dual PCI Buses

The Model 9220 architecture features two 64-bit PCI buses, each capable of 33 MHz or 66 MHz speeds. This multiple bus design offers the user a great deal of flexibility in both I/O configuration and bus speed.

PMC Site 1 uses PCI Bus 1 and PMC Sites 2 and 3 use PCI Bus 2. A PCI bridge joins these two buses, while a second PCI bridge connects PCI Bus 1 to the baseboard. Since buses joined by bridges can operate at different speeds, this architecture allows a 66 MHz PMC module mounted in PMC Site 1 to be mixed with slower modules while maintaining 66 MHz operation.

P2 Connectivity

Model 9220 provides connectivity from the P4 connector of PMC Site 3 to rows A and C of the VME backplane P2 connector. This wiring supports both single-ended signals and differential signal pairs. In addition, the P4 connector of PMC Site 2 is optionally connected to rows Z and D of the VME backplane P2 connector.

Connectivity Between PMC Sites

Connectivity between the P4 connectors of PMC sites 1 and 2 on the 9220 is optionally available. This allows communication between PMC modules offering P4 I/O, such as Pentek's 7131, 7140 and 7142 A/D and Digital Receiver modules.

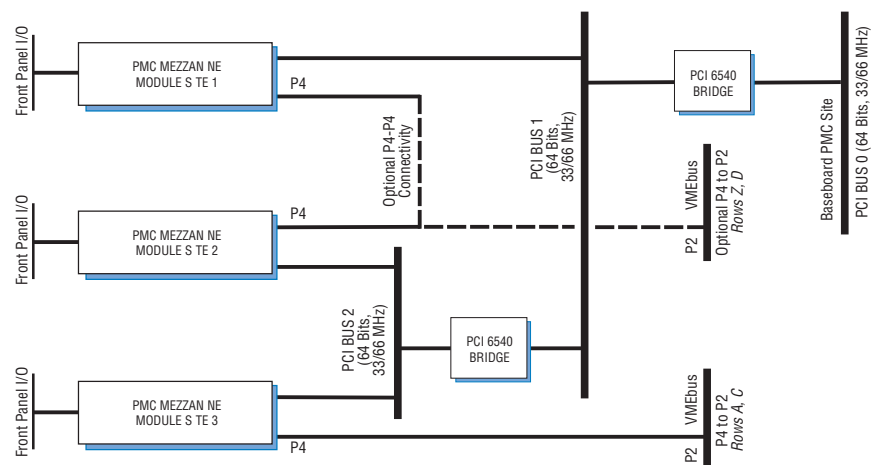
VME Interface

Model 9220 directly connects to the VMEbus to draw power for its on-board power supplies, as well as to support P2 connectivity.

Ordering

Model 9220 can be ordered separately from the baseboard as shown in Ordering Information. Alternatively, for new baseboard orders the 9220 can be factory installed by specifying the following baseboard options: Model 42xx-150 adds the Model 9220 (std) Model 42xx-151 adds the Model 9220-151 Model 42xx-152 adds the Model 9220-152

For example, to order a standard 9220 mounted on a 4205 baseboard, the correct ordering number would be 4205-150.





PENTEK

SYSTEMS AND RECORDERS

SYSTEMS & RECORDERS

MODEL	DESCRIPTION
RTS	Pentek RTS® Real-Time Recording Systems: Flexible and Deployable Instruments
RTS 2701	Rack-mount Real-Time Data Recording and Playback Instrument with Multiband Transceiver
RTS 2703	2-Channel 200 MSample/sec Real-Time Recorder Instrument
RTS 2711	Dual-channel 500 Megasamples-per-second Real-time Data Recorder Instrument
RTS 2721	Portable Multiband Recording and Playback Instrument
	Customer Information

[Click Here for the PRODUCT SELECTOR](#)

Last updated: November 2010

Pentek RTS® Real-Time Recording Systems: Flexible and Deployable Instruments



RTS Systems Include:

- Pentek SystemFlow® recording software with graphical user interface
- SystemFlow virtual oscilloscope and spectrum analyzer
- SystemFlow API
- Complete high performance Windows® workstation
- Time stamping support
- Detailed technical documentation

RTS Systems Benefits:

- Complete turnkey instruments
- Portable, rack-mount and desktop form factors
- Sustained recording rates to 1 GB/sec
- Recordings to NTFS file system for easy and immediate file access
- Supported RAID levels of 0, 1, 5, 6, 10 and 50
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom

The RTS Real-Time Recording Systems eliminate the time and risk associated with new technology system development. With increasing pressure in both the defense and commercial arenas to get to the market first, today's system engineers are looking for more complete off-the-shelf subsystem offerings.

Out of the box, all RTS systems arrive as complete instruments with a full-featured virtual operator control panel ready for immediate data recording and/or playback operation. Because they consist of modular COTS board-level products and flexible control software, they are easily scalable to larger multichannel data acquisition and recording applications requiring sustained, aggregate recording rates of up to 1 GB/sec. For example, they can be used as the data acquisition resource for embedded systems in real-time digital signal processing applications. A complete suite of software development tools simplifies custom system integration.

Ready-to-Run Recording Instruments

The RTS offerings are complete, fully integrated instruments featuring a range of A/D and D/A resources with high-speed disk arrays.

Since RTS instruments are built on a Windows workstation, users can easily install post-processing and analysis tools to operate on the recorded data.

Pentek's RTS systems provide a flexible architecture that can be easily customized to meet user needs. Multiple RAID levels of 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy.

SystemFlow Recording Software

All RTS recording systems are supported with the Pentek SystemFlow Recording

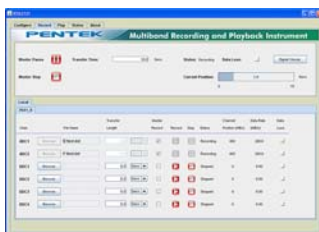
Software suite. SystemFlow provides a rich set of features for controlling the data acquisition and recording functionality of these instruments and ensures a consistent look and feel for developers across all RTS systems.

SystemFlow's GUI (graphical user interface) allows the operator to control all programmable hardware function parameters including gating, triggering, data formatting and clock selection on the various A/D, D/A, DDC (digital downconverter) and DUC (digital upconverter) modules.

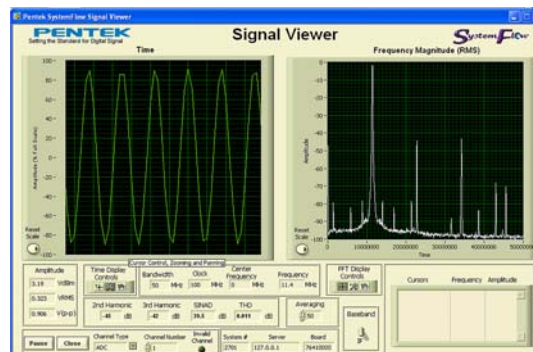
The NTFS file management system supports recording and playback of data files on disk arrays with up to four terabytes of storage. Configuration profiles for specific hardware settings can be stored and retrieved to streamline setting up recurring measurement scenarios. Using the NTFS file system provides for immediate access to recorded data as opposed to systems using proprietary file systems.

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

The SystemFlow API allows developers to configure and customize the subsystem interfaces and operation. Source code is supplied for all client API functions. A well-defined set of plug-ins allows the user to extend server API functions.



Recorder Interface



Signal Viewer



Hardware Configuration

New!

Model RTS 2701

Rack-mount Real-Time Data Recording and Playback Instrument with Multiband Transceiver



SystemFlow

Features

- Complete dual channel transceiver recording and playback system
- 19 inch industrial rack-mount PC server chassis
- Complete high performance Windows® workstation
- Two 14-bit 125 MHz A/Ds
- One 16-bit 500 MHz D/A
- Real-time sustained recording rates of up to 480 MBytes/sec
- 4 terabytes of storage to NTFS RAID disk array
- RAID levels 0, 1, 5, 6, 10 and 50
- Windows SystemFlow® Record/Playback software
- Complete GUI with Signal Viewer analysis tool which includes a virtual oscilloscope and spectrum analyzer
- File headers include time stamping and recording parameters
- DDC decimation and DUC interpolation range from 2 to 32,768
- 8 kHz to 60 MHz baseband record and playback signal bandwidths
- IF frequencies to 300 MHz
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom

Contact factory for options, for number and type of analog channels, recording rates, and disk capacity.

General Information

The Pentek RTS 2701 is a turnkey, multi-band recording and playback instrument that allows the user to record and reproduce high-bandwidth signals. The RTS 2701 provides sustained recording rates of up to 480 MB/sec in a dual-channel configuration and is ideal for the user that requires a powerful rack-mount recording system.

The heart of the RTS 2701 is the Pentek Model 7641-420 multiband transceiver, which includes recently introduced A/D and D/A converters, digital upconverters (DUCs), digital downconverters (DDCs), and an FPGA-installed IP core. The architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

SystemFlow Software

Included with this instrument is Pentek's SystemFlow Recording Software. A software API is provided that allows users to integrate control of the RTS instrument into their system.

The RTS 2701 features a Windows-based GUI (graphical user interface) that provides a simple means to configure and control the instrument. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

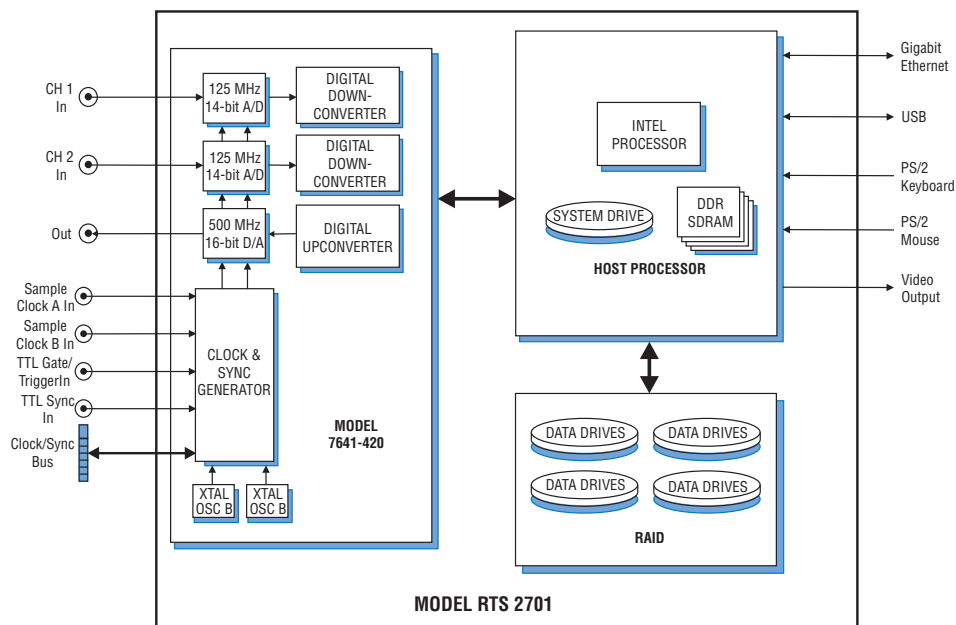
SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows XP Professional workstation, users can install post processing and analysis tools to operate on the recorded data. The RTS 2701 records data to the native NTFS file system, providing immediate access to the recorded data. Data can be offloaded via gigabit Ethernet, or USB 2.0 ports. Additionally, data can be copied to disk, using the 8X double layer DVD +R/RW drive.

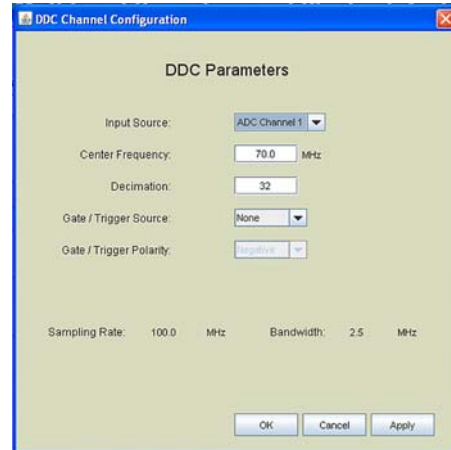
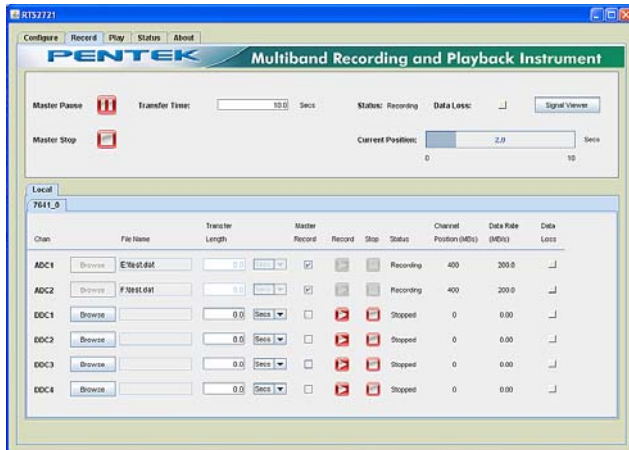
Flexible Architecture

Pentek's multiband recorder instrument provides a flexible architecture that is easily customized to meet the user's needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the level of redundancy that's required. Total drive capacity is 4 TB using 10 drives.

The system supports simultaneous recording of one or two wideband A/D or multiband DDC channels. The analog output allows a single recorded signal to be reproduced as either a baseband or an upconverted IF signal. With its range of programmable decimation and interpolation factors, the system supports signal bandwidths from 8 kHz to 60 MHz. ➤



SystemFlow Graphical User Interface

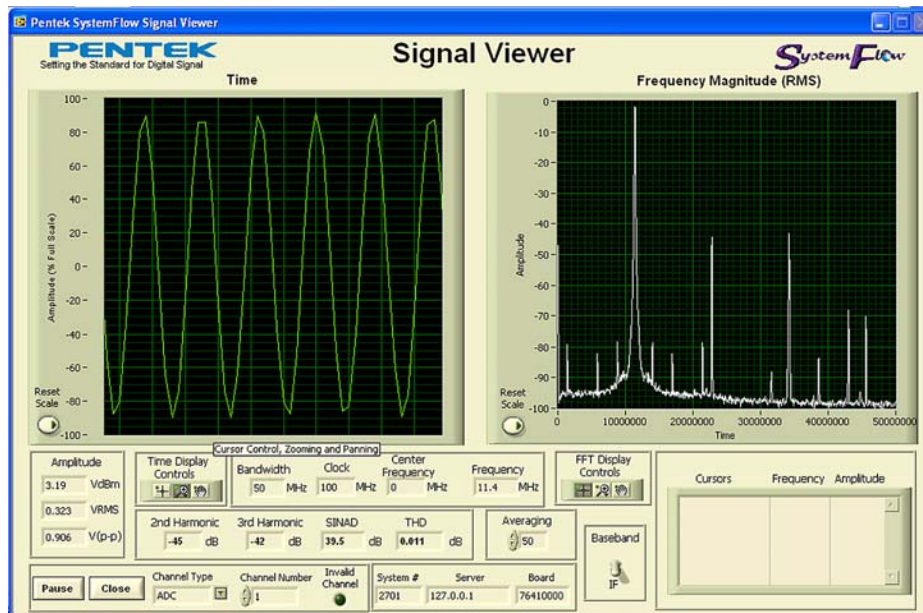


SystemFlow Recorder Interface

The RTS 2701 GUI provides the user with a control interface for the recording instrument. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

SystemFlow Hardware Configuration Interface

The RTS 2701's configuration screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.



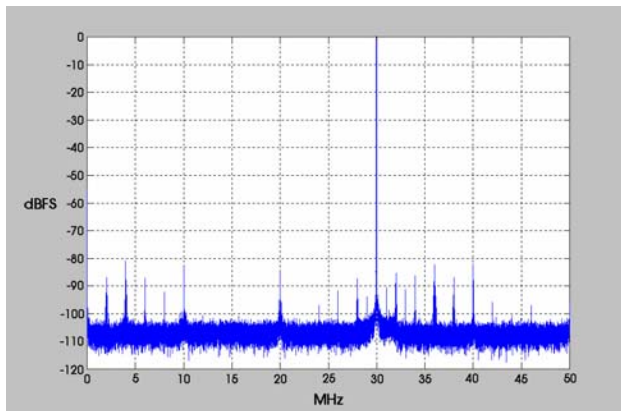
SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

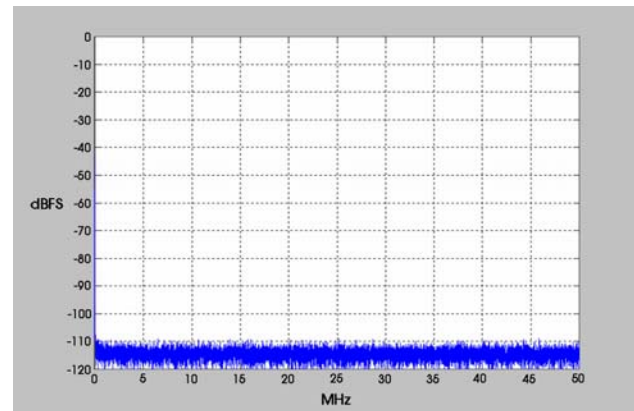
Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

A/D Performance

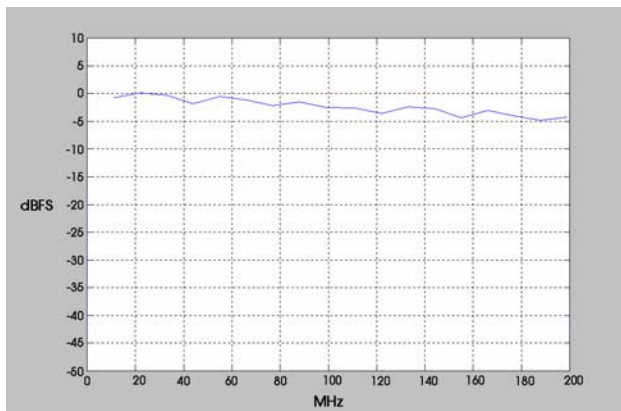
Spurious Free Dynamic Range


 $f_{in} = 70 \text{ MHz}, f_s = 100 \text{ MHz}$

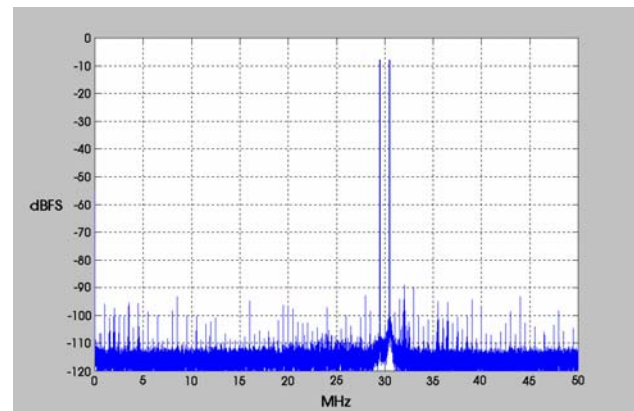
Spurious Pickup


 $f_s = 100 \text{ MHz}, 32k \text{ point FFT}, 8 \text{ averages}$

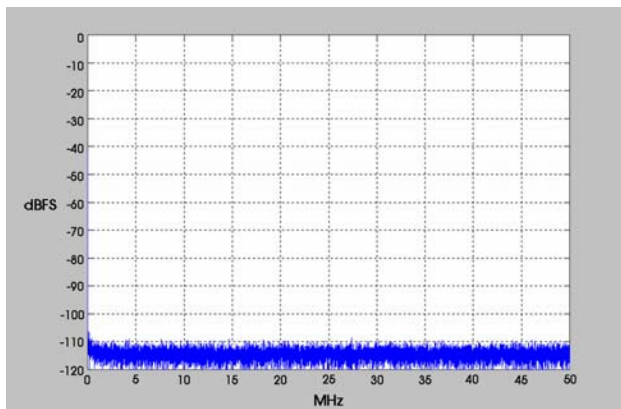
Input Frequency Response


 $f_s = 100 \text{ MHz}$

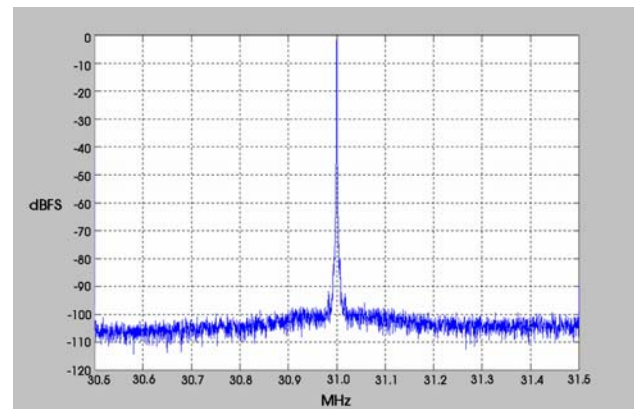
Two-Tone SFDR


 $f_1 = 29.5 \text{ MHz}, f_2 = 30.5 \text{ MHz}, f_s = 100 \text{ MHz}$

Crosstalk


 $f_{in \text{ Ch2}} = 69 \text{ MHz}, f_s = 100 \text{ MHz}, \text{Ch 1 shown}$

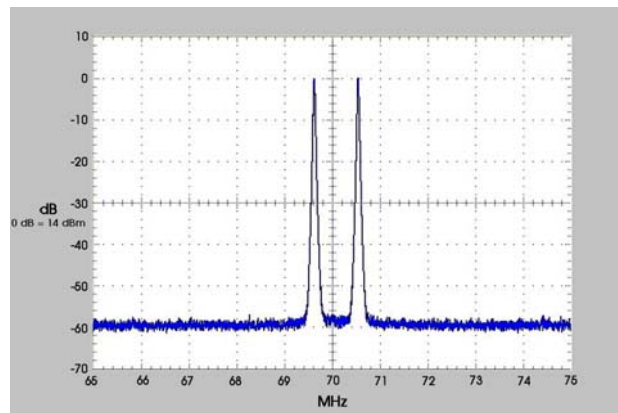
Phase Noise


 $f_{in} = 69 \text{ MHz}, f_s = 100 \text{ MHz}$

Phase Noise @ 100 kHz = $-102 - 10 \cdot \log(610) = -129.8 \text{ dB/Hz}$

D/A Performance

Two-Tone Intermodulation Distortion



$$f_1 = 69.5 \text{ MHz}, f_2 = 70.5 \text{ MHz}, f_s = 100 \text{ MHz}$$

Specifications

PC Workstation (standard configuration)

Operating System: Windows XP Pro

Processor: Intel processor

Speed: 1.8 GHz or greater

SDRAM: 2 GBytes

RAID

Storage: 4 TB

Number of Drives: 10

Supported Levels: 0, 1, 5, 6, 10 and 50

Analog Recording Input / Output

Analog Signal Inputs

Quantity: 2

Input Type: Transformer-coupled, front panel female MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technologies LTC2255

Sampling Rate: 1 MHz to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016 and Pentek installed DDC IP Core

Number of Channels: 4

Decimation: 2 to 32,768

Bandwidth: 8 kHz to 60 MHz

Analog Signal Outputs

Quantity: 1

Output Type: Transformer-coupled, front panel female MMCX connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686 and Pentek installed interpolation IP core

Interpolation: 2 to 32,768

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max.; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (2): Selectable from onboard 100 and 200 MHz crystal oscillators, external or LVDS clocks (Option -136)

External Clocks (2)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 1 to 125 MHz

Multi-Recorder Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Physical and Environmental

Size: 19" W x 21" D x 7" H

Weight: 60 lb

Operating Temp: 0° to 50° C

Storage Temp: -40° to 100° C

Relative Humidity: 5 to 95%, non-cond.

Specifications are subject to change without notice.

Sample Storage Configurations							
Record Mode	Number of Channels	RAID Level	A/D Sample Rate	DDC Decimation	Max. Recorded Signal Bandwidth*	Total Storage Capacity	Total Record Time
A/D	2	0	120 MHz	n/a	60 MHz	4 TB	127 min.
A/D	2	0	100 MHz	n/a	50 MHz	4 TB	166 min.
A/D	2	5	100 MHz	n/a	50 MHz	4 TB	166 min.
A/D	1	0	125 MHz	n/a	62.5 MHz	2 TB	133 min.
DDC	2	0	125 MHz	8	12.5 MHz	4 TB	8.8 hrs.
DDC	2	5	100 MHz	32	2.5 MHz	4 TB	44 hrs.

* For A/D outputs: Bandwidth = $f_s/2$ (Nyquist rate); for DDC outputs: Bandwidth = $80\% * f_s/\text{Decimation factor}$

New!

Model RTS 2703

2-Channel 200 MSample/sec Real-time Recorder Instrument



SystemFlow

Features

- Complete dual channel recording system
- 19 inch 4U industrial rack-mount PC server chassis
- Complete high performance Windows® XP workstation
- Digitizes two analog inputs each at sampling rates to 200 Msamples/sec
- Two 16-bit 200 MHz A/D converters
- Real-time aggregate sustained recording rates up to 800 MByte/sec
- 4 terabytes of storage to NTFS RAID disk array
- Hot-swap SATA drives
- RAID levels 0, 1, 5, 6, 10, and 50
- Windows SystemFlow® Recording software
- Complete GUI with Signal Viewer analysis tool which includes a virtual oscilloscope and spectrum analyzer
- File headers include time stamping and recording parameters
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom

Contact factory for options, for number and type of analog channels, recording rates, and disk capacity.

General Information

The Pentek RTS 2703 is a turnkey recording instrument that allows the user to record and analyze two high-bandwidth signals. The RTS 2703 provides sustained, aggregate recording rates of up to 800 MB/sec, forming a powerful dual-channel 4U rack-mount recording system.

The front end of the RTS 2703 consists of two Pentek Model 7850 PCIe modules each equipped with 200 MHz 16-bit A/D converters. The RTS 2703 retains all 16 bits of each A/D sample (2 bytes), recording two signals at up to 200 MSamples/sec.

A total of 4 TB of RAID storage is provided, allowing sustained 2 TB recordings at 200 MSamples/sec simultaneously on each of two channels for over one hour.

SystemFlow Software

Included with this instrument is Pentek's SystemFlow Recording Software. A software API allows users to integrate control of the RTS instrument into larger system applications.

The RTS 2703 features a Windows-based GUI (graphical user interface) providing a simple means to configure and control the instrument. Custom configurations can be stored as profiles and later retrieved for easy selection of pre-configured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

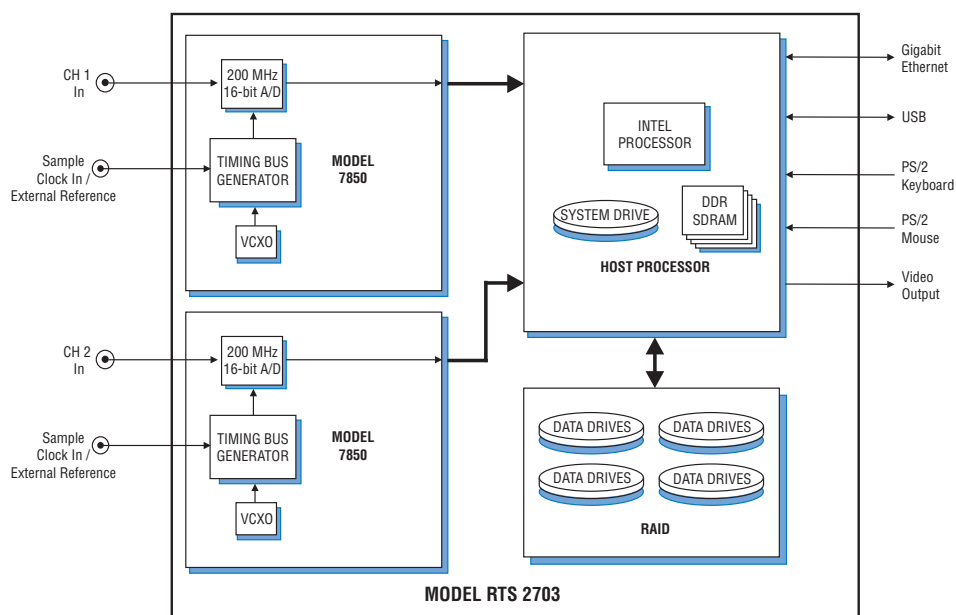
Built on a Windows XP Professional workstation, users can install post processing and analysis tools to operate on the recorded data. The RTS 2703 records data to the native NTFS file system, providing immediate access to the recorded data.

Recorded data can be offloaded from the RTS 2703 via gigabit Ethernet, or USB 2.0 ports. Additionally, data can be copied to an optical disk, using the 8X double layer DVD ±R/RW drive on the front panel.

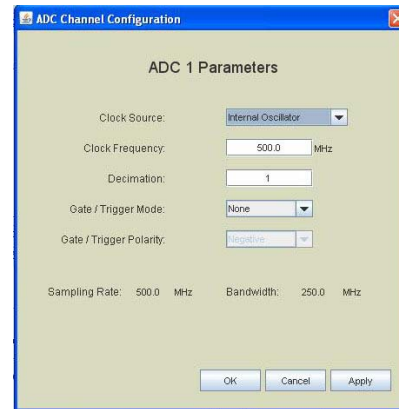
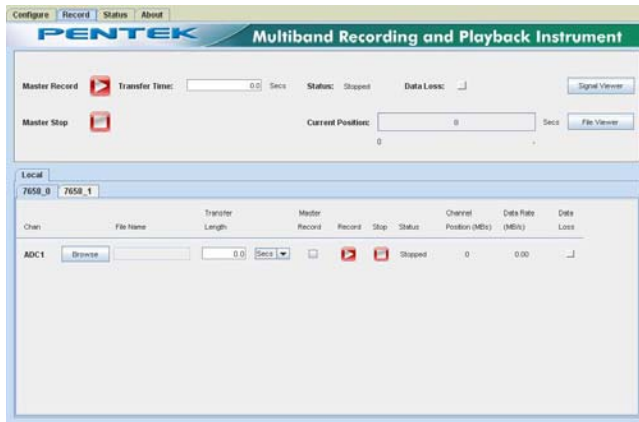
Flexible Architecture

Pentek's RTS 2703 provides a flexible architecture that can be easily customized to meet user needs. Multiple RAID levels, including 0, 1 and 5, provide a choice for the required level of redundancy. The total drive capacity is 4 TB using 10 drives, which are organized as two 5-drive, 2 TB arrays, one array for each A/D channel.

Channels can easily be added to a recording system by adding more RTS 2703 chassis. The SystemFlow software provides the capability of configuring and controlling multiple RTS 2703's, enabling scalable channel count and drive capacity. ➤



SystemFlow Graphical User Interface

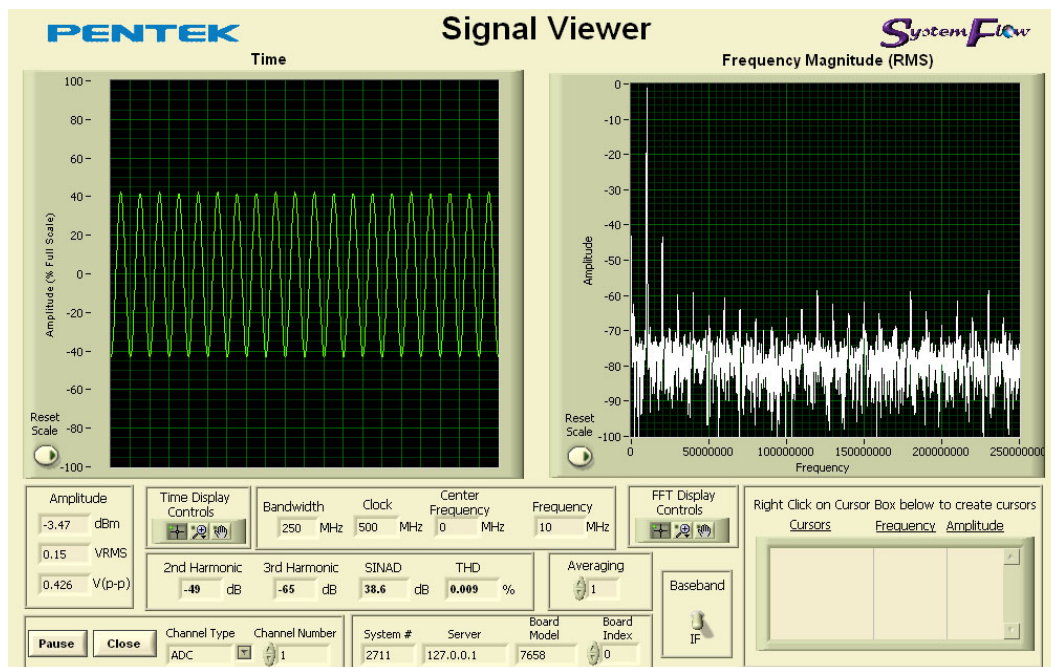


SystemFlow Recorder Interface

The RTS 2703 GUI provides the user with a control interface for the recording instrument. It includes Configuration, Record, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or analyze recorded signals on disk.

SystemFlow Hardware Configuration Interface

The RTS 2703's configuration screens provide a simple and intuitive means for setting up the system parameters. The ADC configuration screen shown here, provides entries for clock selection, decimation and triggering. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.



SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes, and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

Clocking and Synchronization

The RTS 2703 contains two Model 7850 PCIe modules, each providing one 200 MHz 16-bit A/D converter and a 200 MHz oscillator used as the A/D sample clock for each module.

For synchronous operation across the two channels, a timing cable connects between the two 7850 modules ensuring synchronous clocking, gating and triggering operations between the two A/D channels. One 7850 acts as the timing master and the other as the slave.

In the synchronous mode, the 200 MHz oscillator of the master supplies the sample clock for both channels. If the master 7850 is configured to accept an external sample clock, it is used as the sample clock for both channels. Additionally, the gate, trigger and sync signals from the master also control the slave.

Specifications

PC Workstation

Operating System: Windows XP Pro

Processor: Intel Dual Xeon processor

Speed: 1.8 GHz or greater

SDRAM: DDR3, 2 GBytes

System Drive: 500 GB SATA II

USB 2.0 Ports: Two on front panel, two on rear panel

Ethernet: Two rear panel RJ-45 GigE ports

Optical Drive: DVD/CD R/W

Mouse/Keyboard: Two PS/2 rear panel connectors

Front Panel Controls: Power on/off, system reset, alarm reset

Front Panel Indicators: Power on, system HD active, GigE ports active (2), RAID HDs active (10), alarm

RAID Arrays

Number of RAID Arrays: 2

Number of Drives: 10 total (5 drives per array)

Disk Drive Type: SATA II

Drive Access: Hot-swap, removable via front panel

Indicators: Power (10) and activity (10)

Storage: 4 TB total (2 TB per array)

Supported Levels: 0, 1, 5, 6, 10, and 50

Recording

A/D Sampling Rate: 200 MSamples/sec per channel, maximum (RAID 0)

Aggregate Recording Rate: 800 MS/sec, maximum (2 A/D channels at 200 MS/sec each, 2 bytes/sample, RAID 0)

File Format: NTFS

Length of Recording: More than 1 hour for both channels at 200 MS/sec.

Analog Recording Inputs

Data Acquisition Modules

Type: Pentek Model 7850

Quantity: 2

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 30 MHz to 200 MHz

Resolution: 16 bits

Analog Signal Inputs

Quantity: 2 (Ch 1 inputs on each 7850)

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 250 kHz to 350 MHz

Connectors: Two rear panel SMC connectors

Input Impedance: 50 ohms, transformer-coupled

Transformer Type: Coil Craft WBC1-1TLB

A/D Sample Clock

Internal Sample Clock: Two internal 200 MHz oscillators, one on each 7850

External Sample Clock

Quantity: 2 (Clock In, on each 7850)

Frequency: 30 MHz to 200 MHz

Connectors: Two rear panel SMCs

Input Level: Sine wave, 0 to +10 dBm

Input Impedance: 50 ohms, transformer-coupled

Synchronization: LVPECL timing cable connects two 7850 A/D modules as a master/slave pair, providing identical sample clock, gate/trigger and sync signal to both channels

Physical and Environmental

Chassis: 4U, standard 19-inch rack-mount

Dimensions: 19" W x 26" D x 7" H

Weight: 80 lb

Operating Temp: 0° to 50° C

Storage Temp: -20° to 80° C

Relative Humidity: 5 to 95%, non-cond.

Specifications are subject to change without notice

New!

Model RTS 2711



SystemFlow

Features

- Complete dual channel recording system
- 19 inch 4U industrial rack-mount PC server chassis
- Complete high performance Windows® workstation
- Two 12-bit 500 MHz A/Ds, retaining 8-bit samples for full-rate recording
- Real-time aggregate sustained recording rates up to 1 GB/sec
- 4 terabytes of storage to NTFS RAID disk array
- Hot swap SATA drives
- RAID levels 0, 1, 5, 6, 10 and 50
- Windows SystemFlow® Recording software
- Complete GUI with Signal Viewer analysis tool which includes a virtual oscilloscope and spectrum analyzer
- File headers include time stamping and recording parameters
- Digitizes two analog inputs each at sampling rates to 500 megasamples per second
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom

Contact factory for options, for number and type of analog channels, recording rates, and disk capacity.

Dual-channel 500 Megasamples-per-second Real-time Data Recorder Instrument

General Information

The Pentek RTS 2711 is a turnkey recording instrument that allows the user to record and analyze two high-bandwidth signals. The RTS 2711 provides sustained, aggregate recording rates of up to 1 GB/sec forming a powerful dual-channel 4U rack-mount recording system.

The front end of the RTS 2711 consists of two Pentek Model 7858 PCIe modules equipped with 500 MHz 12-bit A/D converters. The RTS 2711 retains the eight most significant bits of each A/D sample to record two signals at 500 megasamples per second.

A total of 4 TB of RAID storage is provided, allowing sustained 2 TB recordings at 500 megasamples per second simultaneously on each of two channels for over one hour.

SystemFlow Software

Included with this instrument is Pentek's SystemFlow Recording Software. A software API allows users to integrate control of the RTS instrument into larger system applications.

The RTS 2711 features a Windows-based GUI (graphical user interface) that provides a simple means to configure and control the instrument. Custom configurations can be stored as profiles and later retrieved for easy selection of preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

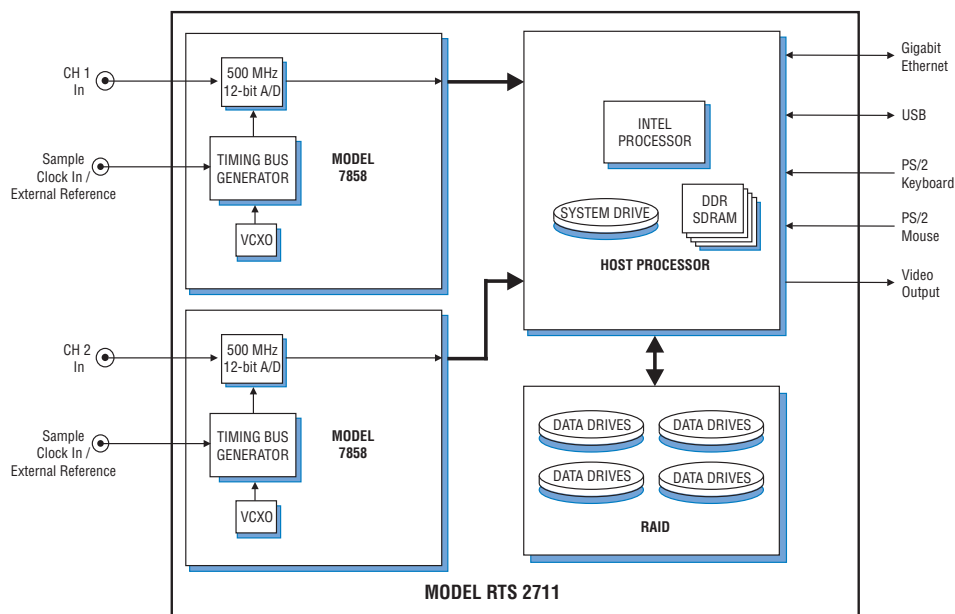
Built on a Windows XP Professional workstation, users can install post-processing and analysis tools to operate on the recorded data. The RTS 2711 records data to the native NTFS file system, providing immediate access to the recorded data.

Recorded data can be offloaded from the RTS 2711 via gigabit Ethernet or USB 2.0 ports. Additionally, data can be copied to disk using the 8X double-layer DVD $\pm$ R/RW drive on the front panel.

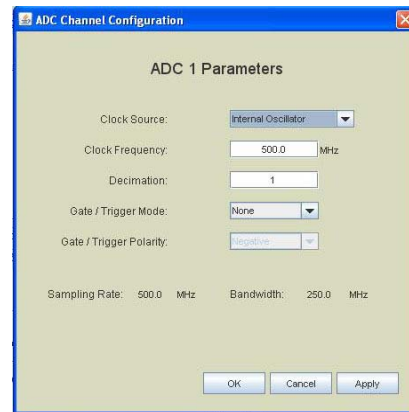
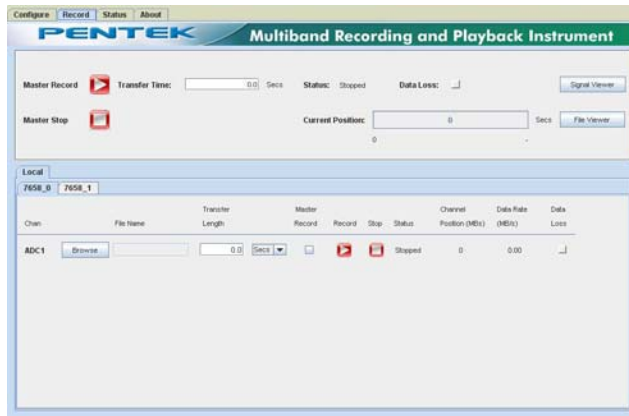
Flexible Architecture

Pentek's RTS 2711 provides a flexible architecture that can be easily customized to meet user needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50 provide a choice for the required level of redundancy. The total drive capacity is 4 TB using 16 drives which are organized as two 8-drive, 2-TB arrays, one for each A/D channel.

Channels can easily be added to a recording system by adding more RTS 2711 chassis. The SystemFlow software provides the capability of configuring and controlling multiple RTS 2711's, enabling scalable channel count and drive capacity ➤



SystemFlow Graphical User Interface

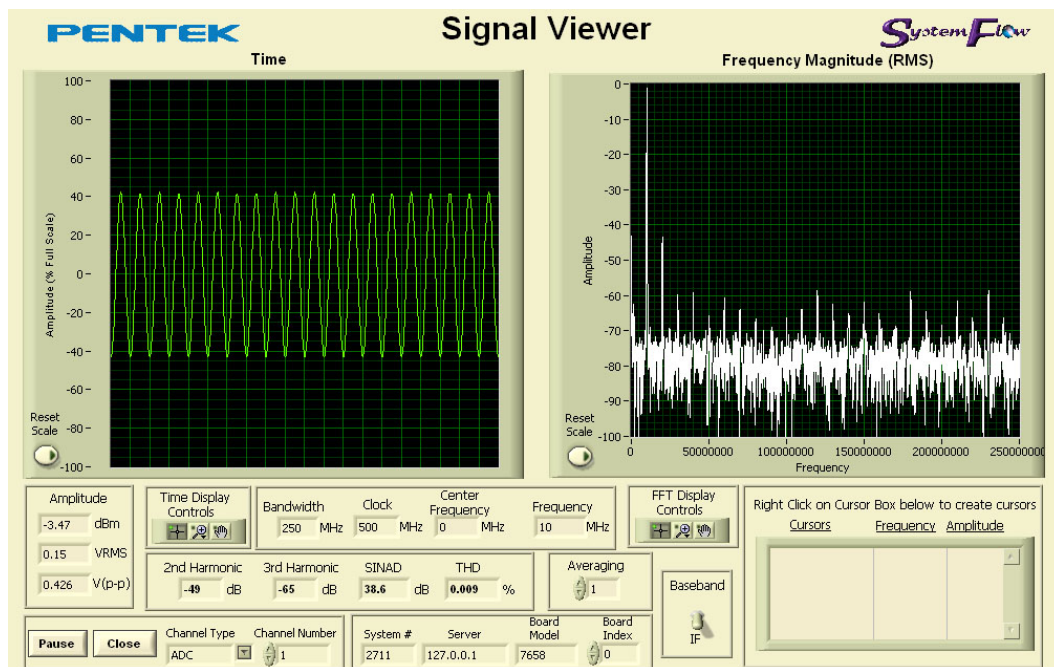


SystemFlow Recorder Interface

The RTS 2711 GUI provides the user with a control interface for the recording instrument. It includes Configuration, Record, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or analyze recorded signals on disk.

SystemFlow Hardware Configuration Interface

The RTS 2711's configuration screens provide a simple and intuitive means for setting up the system parameters. The ADC configuration screen shown here, provides entries for clock selection, decimation and triggering. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.



SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes, and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

Clocking and Synchronization

The RTS 2711 contains two Model 7858 PCIe modules, each providing one A/D converter and a 500 MHz oscillator used as the A/D sample clock for each module. By connecting an external 10 MHz reference clock to both REF IN SMC connectors (one on each module), the two 500 MHz oscillators can be phase-locked to the reference and to each other.

A synchronization cable connected between the two 7858 modules ensures synchronous gating and triggering operations between the two A/D channels.

Specifications

PC Workstation

Operating System: Windows XP Pro
Processor: Intel Dual Xeon processor
Speed: 1.8 GHz or greater
SDRAM: DDR3, 2 GB
System Drive: 500 GB SATA II
USB 2.0 Ports: Two on front panel, two on rear panel
Ethernet: Two rear panel RJ-45 GigE ports
Optical Drive: DVD/CD R/W
Mouse/Keyboard: Two PS/2 rear panel connectors

RAID Arrays

Number of RAID Arrays: 2
Number of Drives: 16 total (eight drives per array)
Disk Drive Type: SATA II
Drive Access: Hot swap, removable via front panel
Storage: 4 TB total (2 TB per array)
Supported Levels: 0, 1, 5, 6, 10 and 50
Recording Rate per A/D Channel: 500 MB/sec max
Aggregate Recording Rate: 1 GB/sec (two A/D channels)
Recording File Format: NTFS

Analog Recording Inputs

Analog Signal Inputs

Quantity: 2

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 250 kHz to 750 MHz

Connectors: Two rear panel SMC connectors

Input Impedance: 50 ohms, transformer-coupled

Transformer Type: Coil Craft WBC1-1TLB

A/D Converters

Type: Texas Instruments ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits with 8 bits retained for recording

Clock Inputs

Internal A/D Clock: Two internal 500 MHz oscillators

External Reference Clock

Operation: Phase-locks both 500 MHz oscillators

Frequency: 10 MHz

Connectors: Two rear panel SMC connectors

Input Level: Sine wave, 0 to +10 dBm

Input Impedance: 50 ohms, transformer-coupled

Physical and Environmental

Chassis: 4U, standard rackmount

Size: 19" W x 26" D x 7" H

Weight: 80 lb

Operating Temp: 0° to 50° C

Storage Temp: -40° to 100° C

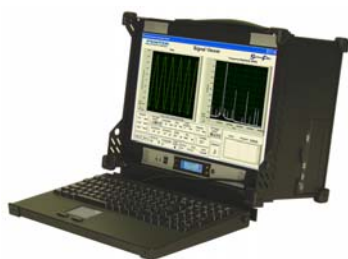
Relative Humidity: 5 to 95%, non-cond.

Specifications are subject to change without notice

New!

Model RTS 2721

Portable Multiband Recording and Playback Instrument



SystemFlow

Features

- Portable system measuring 16.9" W x 9.5" D x 13.4" H
- Lightweight: approximately 30 pounds
- Complete high-performance Windows® workstation
- Two 14-bit 125 MHz A/Ds
- One 16-bit 500 MHz D/A
- Real-time sustained recording rates of up to 480 MB/sec
- Standard configuration with 3 TB of hot-swap storage to NTFS RAID disk array
- RAID levels 0, 1, 5, 6, 10 and 50
- Windows SystemFlow® instrument software
- Complete GUI with Signal Viewer analysis tool which includes a virtual oscilloscope and spectrum analyzer
- File headers include time stamping and recording parameters
- DDC decimation and DUC interpolation range from 2 to 32,768
- 8 kHz to 60 MHz baseband record and playback signal bandwidths
- IF frequencies to 300 MHz
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom

Contact the factory for options, for number and type of analog channels, recording rates, and disk capacity.

General Information

The Pentek RTS 2721 is a turnkey, multi-band recording and playback instrument that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable package. The instrument provides sustained recording rates of up to 480 MB/sec in a dual-channel system and is ideal for the user who requires both portability and performance in a recording system.

The RTS 2721 is supplied in a small footprint portable package measuring only 16.9" W x 9.5" D x 13.4" H and weighing just 30 pounds. With measurements similar to a small briefcase, this portable workstation includes a quad-core Xeon processor, a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

The heart of the RTS 2721 is the Pentek Model 7641-420 multiband transceiver which includes A/D and D/A converters, DDCs (digital downconverters), DUCs (digital upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey instrument.

SystemFlow Software

Included with this instrument is Pentek's SystemFlow Recording Software. A software API is provided that allows users to integrate control of the RTS instrument into their system.

The RTS 2721 features a Windows-based GUI (graphical user interface) that provides a simple means to configure and control the instrument. Custom configurations can be stored as profiles and later loaded

when needed, allowing the user to select preconfigured settings with a single click.

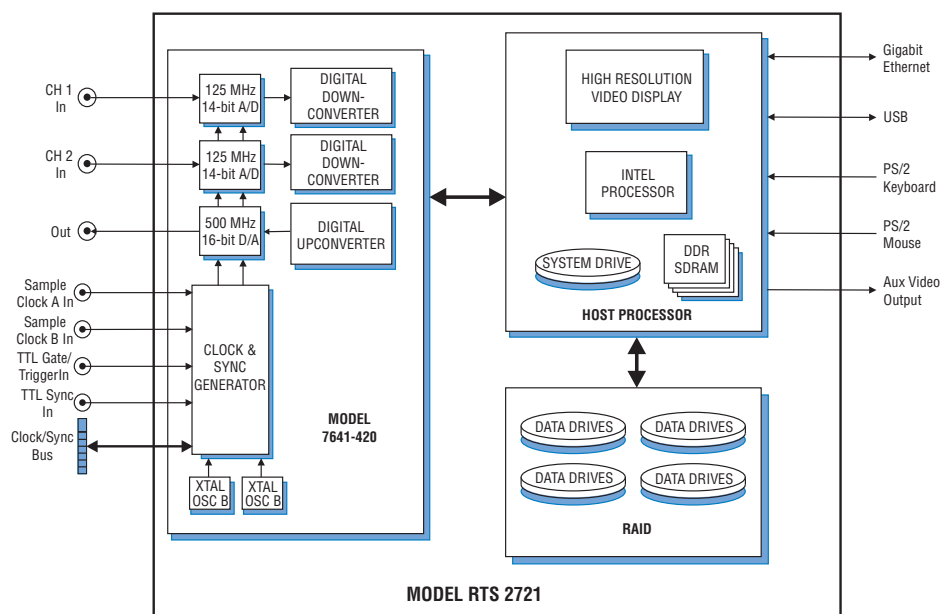
SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Since it's built on a Windows XP Professional workstation, users can easily install post-processing and analysis tools. The RTS 2721 records data to the native NTFS file system that provides immediate access to the recorded data. Data can be offloaded via the hot-swap SATA disks, by gigabit Ethernet or USB 2.0. Data can also be copied to disk, using the 8x double layer DVD ±R/RW drive.

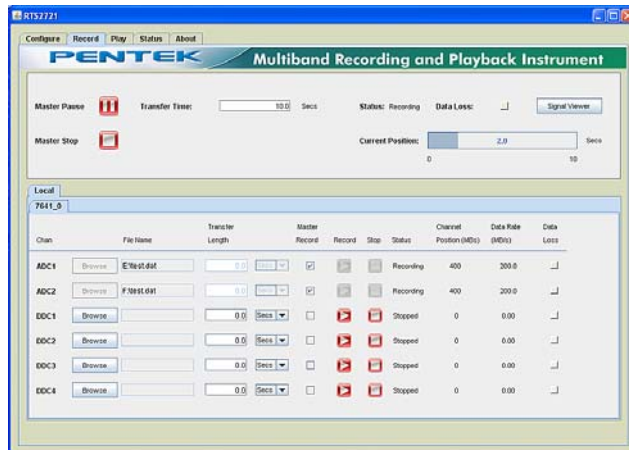
Flexible Architecture

Pentek's portable multiband recorder provides a flexible architecture that is easily customized to meet the user's needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the level of redundancy that's required. Total drive capacity is scalable up to 4.8 TB using as many as 14 hot-swap SATA drives.

The system supports simultaneous recording of one or two wideband A/D or multiband DDC channels. The analog output allows a single recorded signal to be reproduced as either a baseband or an upconverted IF signal. With its range of programmable decimation and interpolation factors, the system supports signal bandwidths from 8 kHz to 60 MHz. ➤



SystemView Graphical User Interface

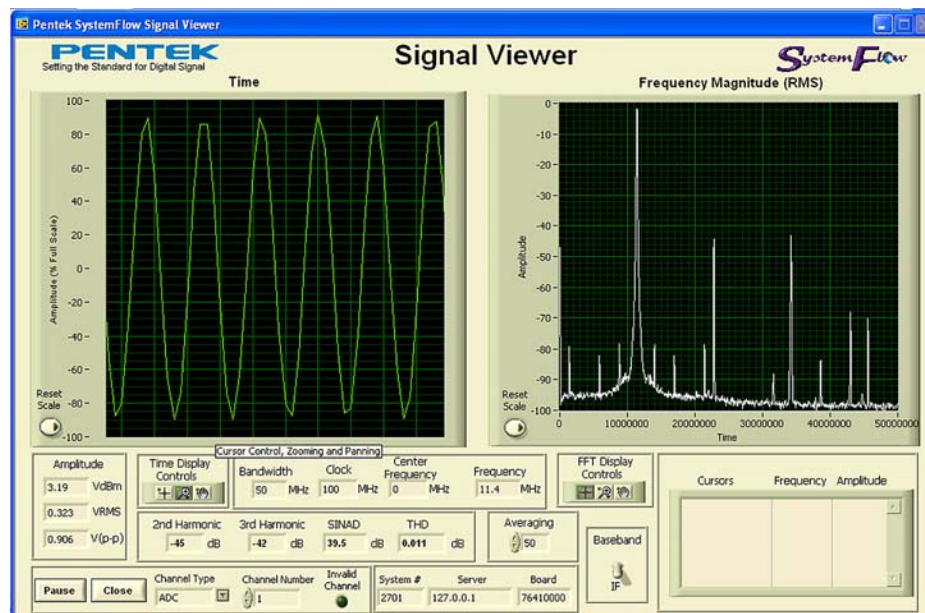


SystemFlow Recorder Interface

The RTS 2721 GUI provides the user with a control interface for the recording instrument. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

SystemFlow Hardware Configuration Interface

The RTS 2721's configuration screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.



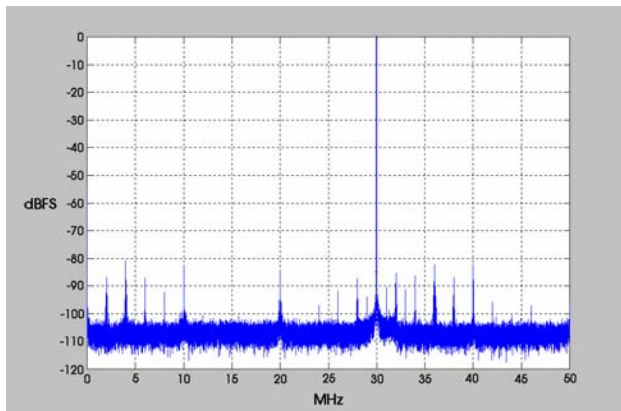
SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

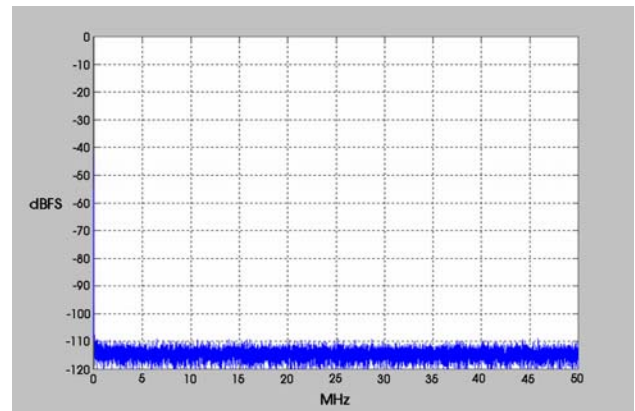
Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

A/D Performance

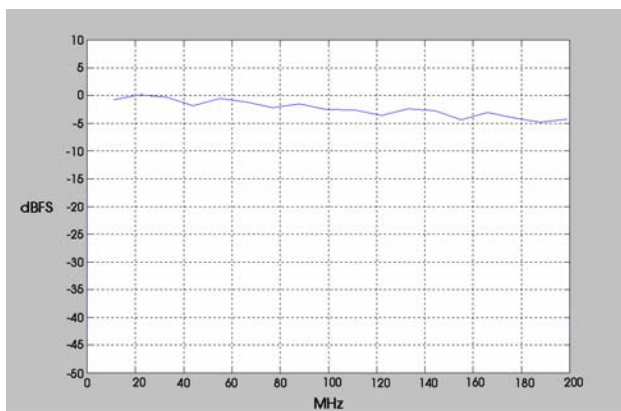
Spurious Free Dynamic Range


 $f_{in} = 70 \text{ MHz}, f_s = 100 \text{ MHz}$

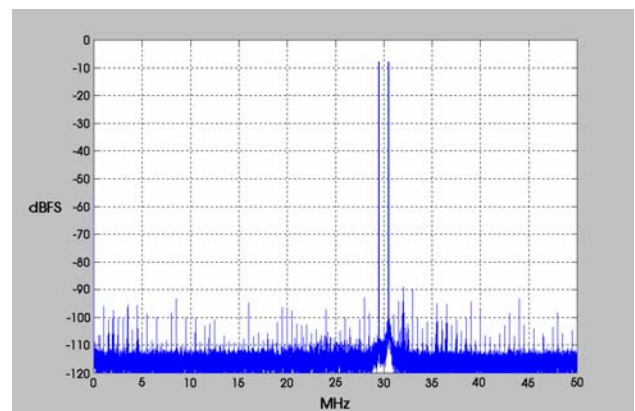
Spurious Pickup


 $f_s = 100 \text{ MHz}, 32k \text{ point FFT}, 8 \text{ averages}$

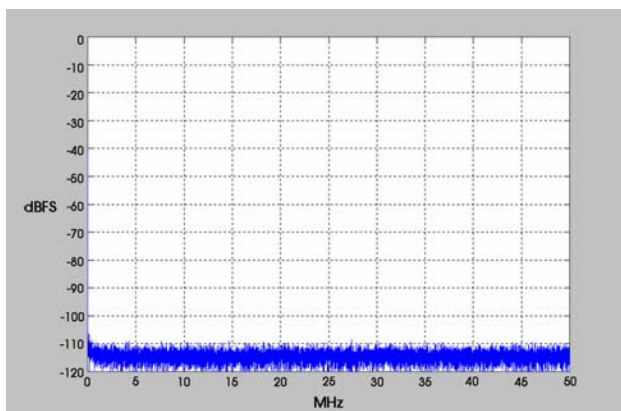
Input Frequency Response


 $f_s = 100 \text{ MHz}$

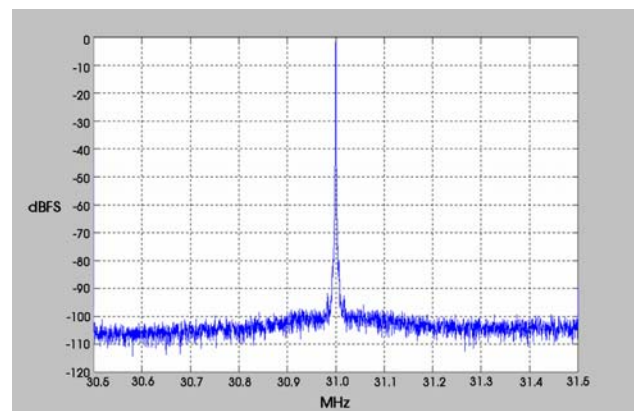
Two-Tone SFDR


 $f_1 = 29.5 \text{ MHz}, f_2 = 30.5 \text{ MHz}, f_s = 100 \text{ MHz}$

Crosstalk

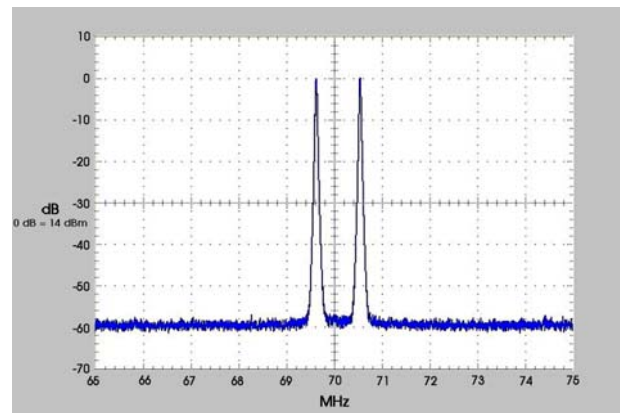

 $f_{in \text{ Ch2}} = 69 \text{ MHz}, f_s = 100 \text{ MHz}, \text{Ch 1 shown}$

Phase Noise


 $f_{in} = 69 \text{ MHz}, f_s = 100 \text{ MHz}$
 $\text{Phase Noise @ } 100 \text{ kHz} = -102 - 10 \cdot \log(610) = -129.8 \text{ dB/Hz}$

D/A Performance

Two-Tone Intermodulation Distortion



$$f_1 = 69.5 \text{ MHz}, f_2 = 70.5 \text{ MHz}, f_s = 100 \text{ MHz}$$

Specifications

PC Workstation (standard configuration)

Operating System: Windows XP Pro

Processor: Intel processor

SDRAM: 2 GB

Monitor: Built-in 17" high-resolution LCD

RAID

Total Storage: 3 TB

Number of Drives: 14

Supported Levels: 0, 1, 5, 6, 10 and 50

Size: 16.9" W x 9.5" D x 13.4" H

Weight: 30 lb

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -25° to 65° C

Relative Humidity: 5 to 95%, non-condensing

Analog Recording Input/Output

Analog Signal Inputs

Quantity: 2

Input Type: Transformer-coupled, front panel female

MMCX connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +10 dBm into 50 ohms

3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technologies LTC2255

Sampling Rate: 1 MHz to 125 MHz

Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016 and Pentek DDC IP Core

Number of Channels: 4

Decimation: 2 to 32,768

Bandwidth: 8 kHz to 60 MHz

Analog Signal Outputs

Quantity: 1

Output Type: Transformer-coupled, front panel female MMCX connector

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 60 kHz to 300 MHz

Digital Upconverter

Type: TI DAC5686 and Pentek interpolation IP core

Interpolation: 2 to 32,768

Input Bandwidth: 40 MHz, max.

Output IF: DC to 160 MHz

Output Signal: Analog, real or quadrature

Sampling Rate: 320 MHz max.; 500 MHz max. with upconversion disabled

Resolution: 16 bits

Clock Sources (2): Selectable from onboard 100 and 200 MHz crystal oscillators, external or LVDS clocks (Option -136)

External Clocks (2)

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 1 to 100 MHz

Multi-Recorder Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Specifications are subject to change without notice.

Sample Storage Configurations							
Record Mode	Number of Channels	RAID Level	A/D Sample Rate	DDC Decimation	Max. Recorded Signal Bandwidth*	Total Storage Capacity	Total Record Time
A/D	2	0	120 MHz	n/a	60 MHz	2.7 TB	90 min
A/D	2	0	100 MHz	n/a	50 MHz	2.7 TB	108 min
A/D	2	5	100 MHz	n/a	50 MHz	2.25 TB	90 min
A/D	1	0	125 MHz	n/a	62.5 MHz	1.35 TB	90 min
DDC	2	0	125 MHz	8	12.5 MHz	2.7 TB	360 min
DDC	2	5	100 MHz	32	2.5 MHz	2.25 TB	25 hr

* For A/D outputs: Bandwidth = $f_s/2$ (Nyquist rate); for DDC outputs: Bandwidth = $80\% * f_s/\text{Decimation factor}$



PENTEK

CLOCK & SYNC GENERATORS

CLOCK & SYNC GENERATORS

MODEL	DESCRIPTION
6890	2.2 GHz Clock, Sync and Gate Distribution Board - VME
6891	System Synchronizer and Distribution Board - VME
7190	Multifrequency Clock Synthesizer - PMC
7290, 7390	Multifrequency Clock Synthesizers - 3U/6U cPCI
7690	Multifrequency Clock Synthesizers - PCI
7790	Multifrequency Clock Synthesizers - x16 PCIe
7890	Multifrequency Clock Synthesizer - x8 PCIe
5390	Multifrequency Clock Synthesizer - 3U VPX
7191	Programmable Multifrequency Clock Synthesizer - PMC
7291, 7391	Programmable Multifrequency Clock Synthesizers - 3U/6U cPCI
7691	Programmable Multifrequency Clock Synthesizers - PCI
7791	Programmable Multifrequency Clock Synthesizers - x16 PCIe
7891	Programmable Multifrequency Clock Synthesizer - x8 PCIe
5391	Programmable Multifrequency Clock Synthesizer - 3U VPX
9190	Clock and Sync Generator for I/O Modules
	Customer Information

Last updated: November 2010



Features

- Synchronizes up to eight separate boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates from 800 MHz to 2.2 GHz
- Front panel SMA connectors for clock input and outputs
- Front panel MMCX connectors for gate/trigger and sync signal inputs and outputs
- Single-slot 6U VME board configuration

Ordering Information

Model	Description
6890	2.2 GHz Clock, Sync and Gate Distribution Board - VME

Accessories

Model	Description
2890-00x	Set of Input and Output Cables for two (-002) to eight (-008) boards

General Information

Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 6890 provides three front panel connectors to accept input signals. One SMA connector is provided for clock signal input, one MMCX connector accepts gate or trigger signals, and another MMCX connector is provided for synchronization. Two additional MMCX connectors are provided for Gate and Sync Enable.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

Clock Signals

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors.

The second output of the 1:2 power splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

Gate and Synchronization Signals

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable MMCX inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.

Accessories

Model 2890 provides various cable sets with options -002 through -008 supporting synchronization of two to eight boards. Options for individual cables are also available under Model 2890.

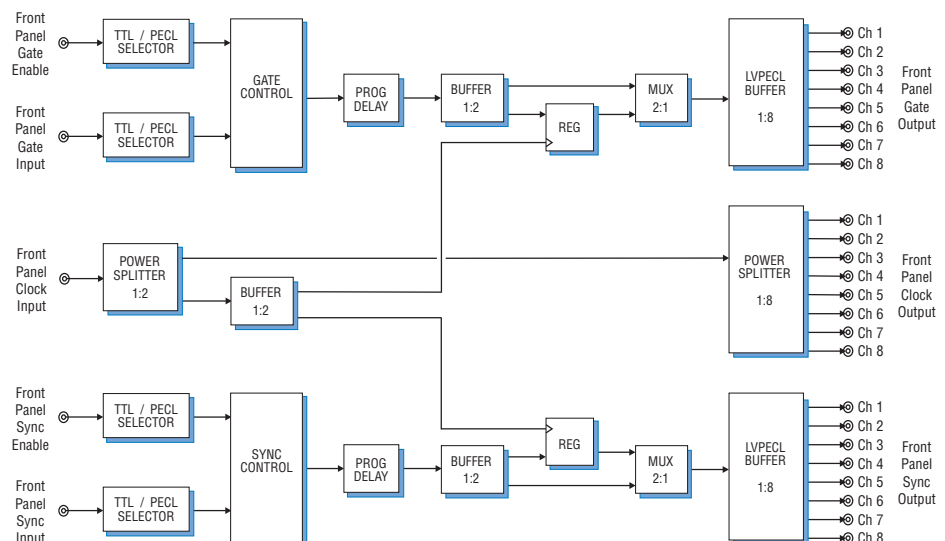
Supported Products

The 6890 currently supports Model 6826 Dual 2 GHz, 10-bit A/D Converter VME Board. Contact the factory for an up-to-date list of supported boards and modules.

Physical Characteristics

Model 6890 is a standard 6U VMEbus board occupying a single VMEbus slot. Dimensions are 160 mm (6.3 inches) deep by 233.5 mm (9.2 inches) high.

The board uses an EMC front panel as specified in IEEE 1101.10. Front panel width is 20.3 mm (0.8 inches).





Features

- Synchronizes up to eight separate I/O modules
- Up to eight 6891's can be linked together to synchronize up to 64 I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 500 MHz
- Front panel SMA connectors for input signals
- Front panel 26-pin Sync Bus connectors compatible with a wide range of Pentek I/O modules
- Single-slot 6U VME board configuration

Ordering Information

Model	Description
6891	System Synchronizer and Distribution Board - VME

Accessories

2891-xxx	Set of Input and Output Cables

General Information

Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions.

For larger systems, up to eight 6891's can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.

Input Signals

Model 6891 provides three front panel SMA connectors to accept TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional SMA connectors are provided for separate gate and sync enable signals.

Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a front panel 26-pin Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

Output Signals

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design.

Clock Signals

The 6891 accepts clock input at +4 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

Gate and Synchronization Signals

The 6891 features separate inputs for gate/trigger and sync signals. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable SMA inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.

Cables

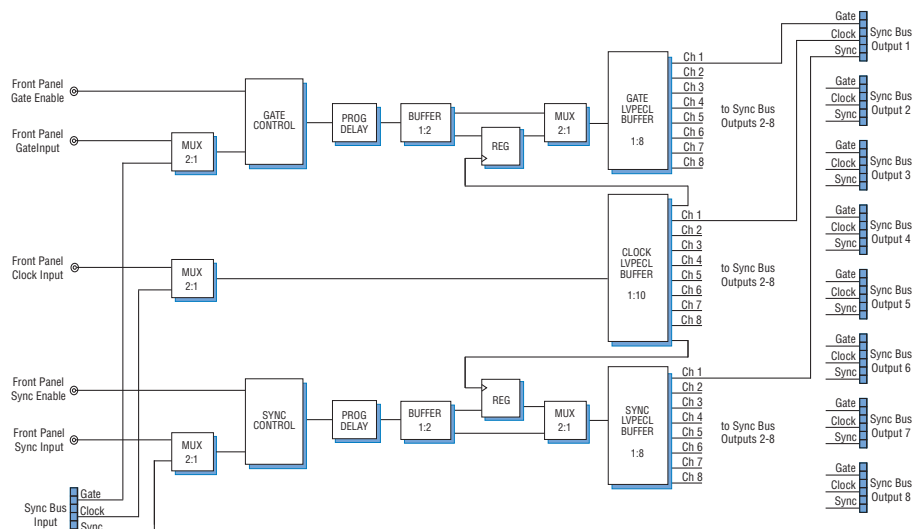
Model 2891 provides various cable kits to support the 6891. Options are available for a range of cable lengths and synchronization of two to eight modules. Options for individual cables are also available under Model 2890.

Supported Products

The 6891 currently supports all models in the 715x family. Contact the factory for an up-to-date list of supported modules.

Physical Characteristics

Model 6890 is a standard 6U VMEbus board occupying a single VMEbus slot.



New!

Model 7190

Multifrequency Clock Synthesizer - PMC



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

General Information

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide

range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7190 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10 \text{ dBm}$

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four)

Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz

Unlocked Accuracy: $\pm 20 \text{ ppm}$

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3 \text{ dBm}$ @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

Environmental

Operating Temp: 0° to 50°C

Storage Temp: -20° to 90°C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.



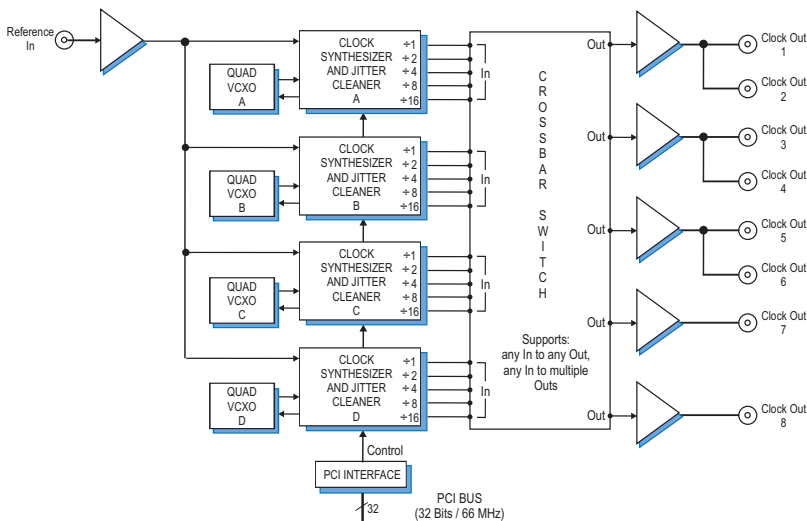
Ordering Information

Model	Description
7190	Multifrequency Clock Synthesizer - PMC

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies



New!

Models 7290, 7290D and 7390

Multifrequency Clock Synthesizers - 3U/6U cPCI



Model 7390 Model 7290D

Features

- Simultaneous synthesis of up to five different clocks
- Eight or 16 SMC clock outputs
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Quad VCXOs allow selection from different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface



Ordering Information

Model	Description
7290	Multifrequency Clock Synthesizer - 6U cPCI
7290D	Dual Multifrequency Clock Synthesizer - 6U cPCI
7390	Multifrequency Clock Synthesizer - 3U cPCI

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

These Models generate up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Models 7290 and 7390 generate eight clocks while Model 7290D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each quad VCXO can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or ten different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where even more different clock outputs are required simultaneously, multiple boards can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

These Models use an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10$ dBm

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four or eight

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four or eight)

Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz

Unlocked Accuracy: ± 20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3$ dBm @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

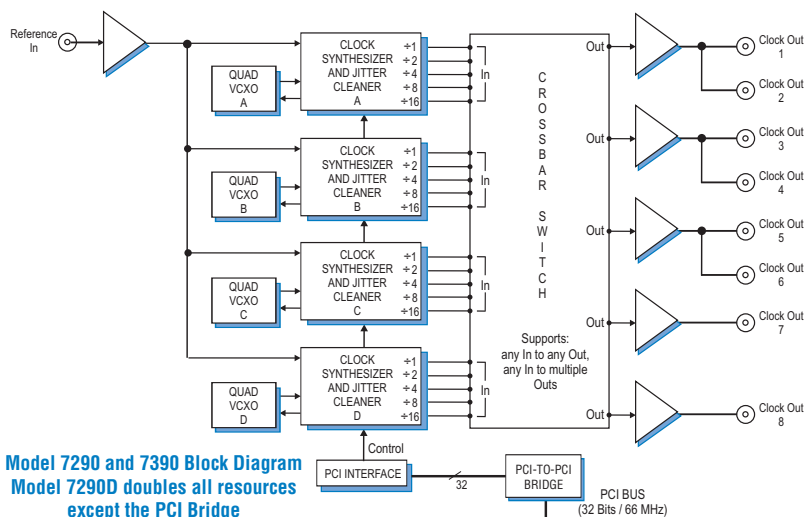
Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board



New!

Model 7690

Multifrequency Clock Synthesizer - PCI



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

General Information

Model 7690 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7690 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7690 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide

range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7690's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7690 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. It attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10$ dBm

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: 4)

Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz

Unlocked Accuracy: ± 20 ppm

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3$ dBm @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board



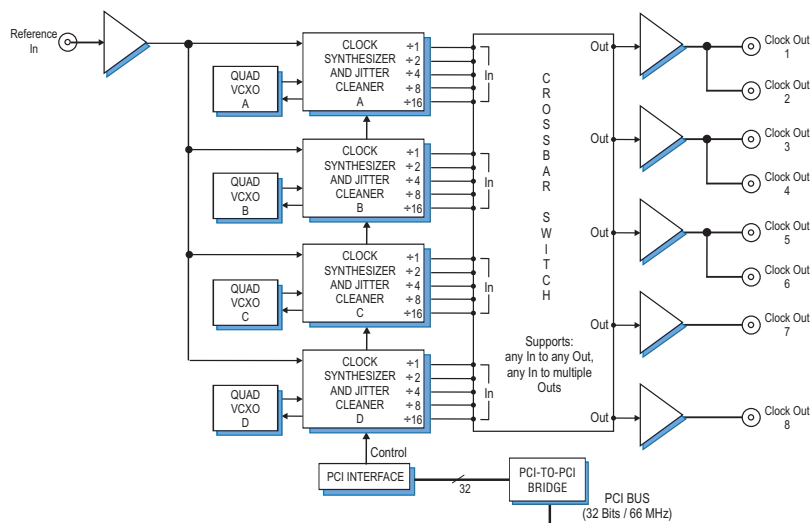
Ordering Information

Model	Description
7690	Multifrequency Clock Synthesizer - PCI

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

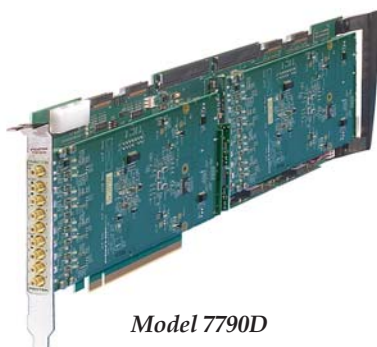
* Contact Pentek to order specific frequencies



New!

Models 7790, 7790D

Multifrequency Clock Synthesizers - x16 PCIe



Model 7790D

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: $-105 \text{ dBc/Hz @ } 1 \text{ kHz offset}$
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface



Ordering Information

Model	Description
7790	Multifrequency Clock Synthesizer - Full-length x16 PCIe
7790D	Dual Multifrequency Clock Synthesizer - Full-length x16 PCIe

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters.

These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to a reference source.

Model 7790 generates eight clocks while Model 7790D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each quad VCXO can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or ten different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where even more different clock outputs are required simultaneously, multiple boards can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

These Models include a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: $-6 \text{ dBm to } +10 \text{ dBm}$

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four or eight

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four or eight)

Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz

Unlocked Accuracy: $\pm 20 \text{ ppm}$

Front Panel Clock Outputs (Quantity: 8 or 16)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3 \text{ dBm @ } 700 \text{ MHz}$

Typ. Phase Noise: $-105 \text{ dBc/Hz @ } 1 \text{ kHz}$ (dependent on reference source stability)

PCI to PCIe Interface

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port to PCI bus, one x16 port to PCIe motherboard

Operation: control and status interface

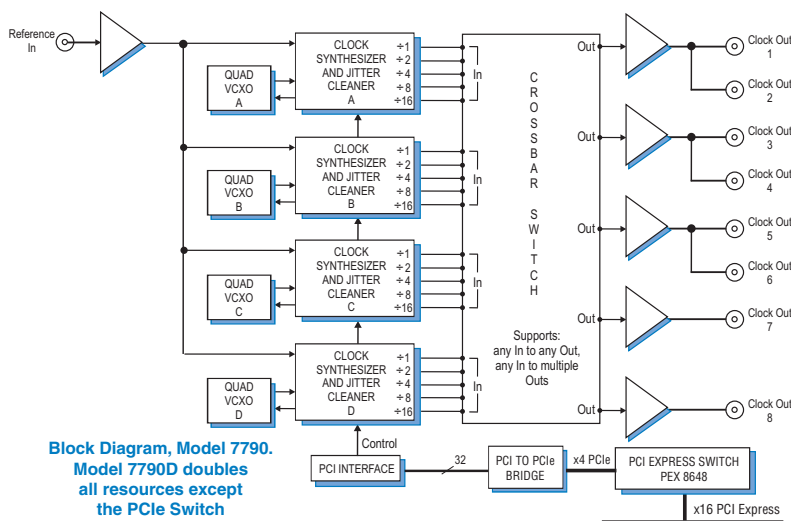
Environmental

Operating Temp: $0^\circ \text{ to } 50^\circ \text{ C}$

Storage Temp: $-20^\circ \text{ to } 90^\circ \text{ C}$

Relative Humidity: 0 to 95%, non-cond.

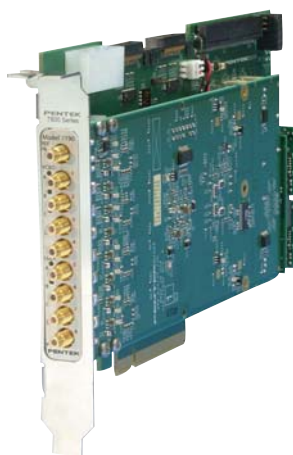
Size: Full-length PCIe, 4.38 in. x 12.3 in.



New!

Model 7890

Multifrequency Clock Synthesizer - x8 PCIe



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

General Information

Model 7890 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7890 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7890 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide

range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7890's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

The Model 7890 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10 \text{ dBm}$

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four)

Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz

Unlocked Accuracy: $\pm 20 \text{ ppm}$

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3 \text{ dBm}$ @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI bus, one x8 port to PCIe motherboard

Operation: control and status interface

Environmental

Operating Temp: 0° to 50°C

Storage Temp: -20° to 90°C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in



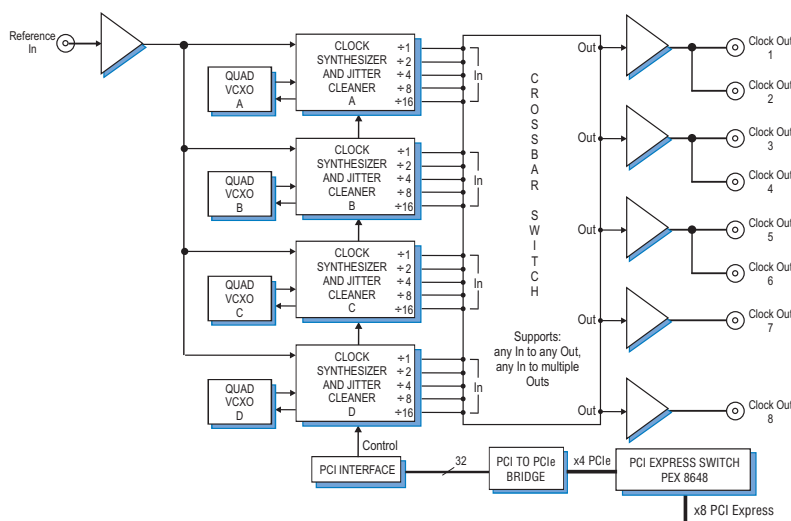
Ordering Information

Model	Description
7890	Multifrequency Clock Synthesizer - Half-length x8 PCIe

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies



New!

Model 5390

Multifrequency Clock Synthesizer - 3U VPX



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane



Ordering Information

Model	Description
5390	Multifrequency Clock Synthesizer - 3U VPX

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

Model 5390 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 5390 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 5390 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to

five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 5390's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Switch

Model 5390 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10 \text{ dBm}$

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four)

Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz

Unlocked Accuracy: $\pm 20 \text{ ppm}$

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3 \text{ dBm}$ @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

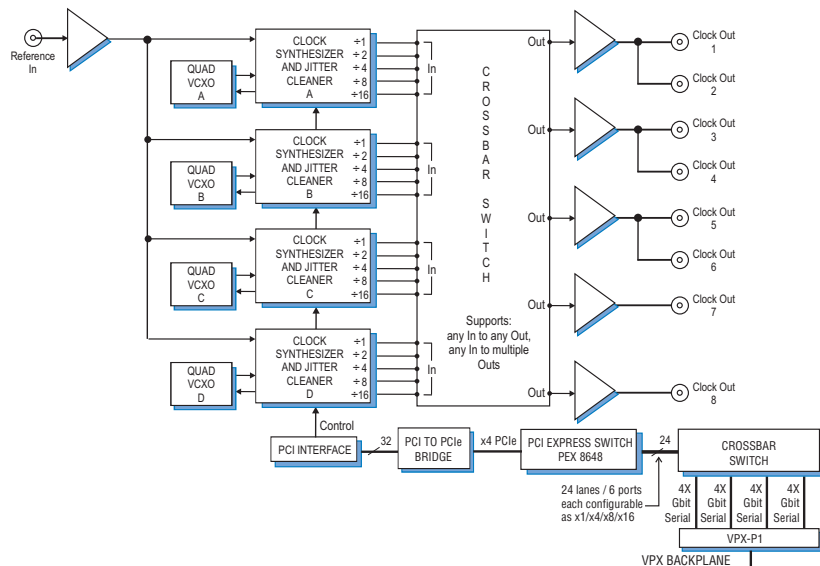
Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)



New!

Model 7191

Programmable Multifrequency Clock Synthesizer - PMC



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

General Information

Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7191 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10 \text{ dBm}$

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: Four)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: $\pm 20 \text{ ppm}$

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3 \text{ dBm}$ @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

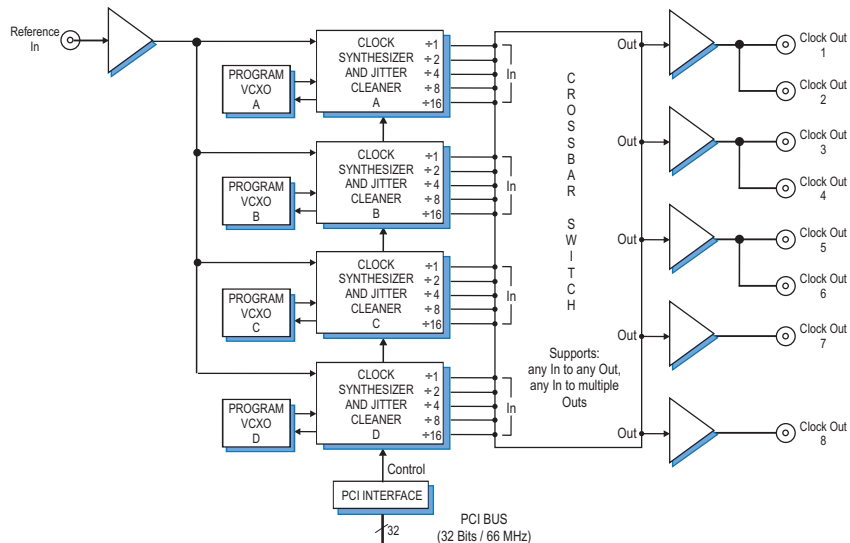
Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

ReadyFlow
Board Support Package

Ordering Information

Model	Description
7191	Programmable Multifrequency Clock Synthesizer - PMC



New!

Models 7291, 7291D and 7391

Programmable Multifrequency Clock Synthesizers - 3U/6U cPCI



Model 7391 Model 7291D

Features

- Simultaneous synthesis of five or ten different clocks
- Eight or 16 SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface



Ordering Information

Model	Description
7291	Programmable Multifrequency Clock Synthesizer - 6U cPCI
7291D	Dual Programmable Multifrequency Clock Synthesizer - 6U cPCI
7391	Programmable Multifrequency Clock Synthesizer - 3U cPCI

General Information

These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. Models 7291 and 7391 generate eight clocks while Model 7291D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO (Voltage Controlled Crystal Oscillator) to provide the base frequency for the clock synthesizer. Each of the VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 or 40 frequencies to the board's output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five or ten clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to 16 different clocks to various outputs.

With independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where more than ten different clock outputs are required simultaneously, multiple 7291D's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

These Models use an industry-standard 32 bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four or eight

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: 4 or 8)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: ± 20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: +3 dBm @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

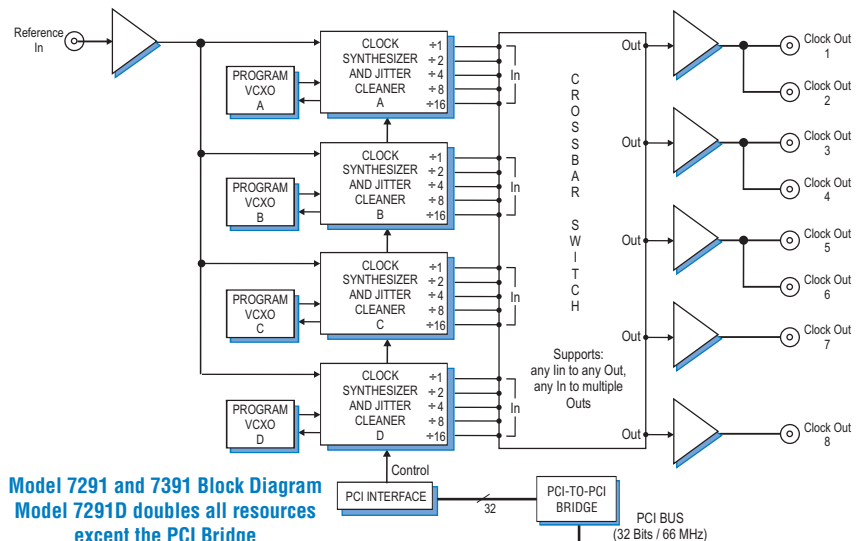
Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board.



Model 7291 and 7391 Block Diagram
Model 7291D doubles all resources
except the PCI Bridge

New!

Model 7691

Programmable Multifrequency Clock Synthesizer - PCI



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

General Information

Model 7691 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7691 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7691 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7691's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7691 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10 \text{ dBm}$

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: Four)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: $\pm 20 \text{ ppm}$

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3 \text{ dBm}$ @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

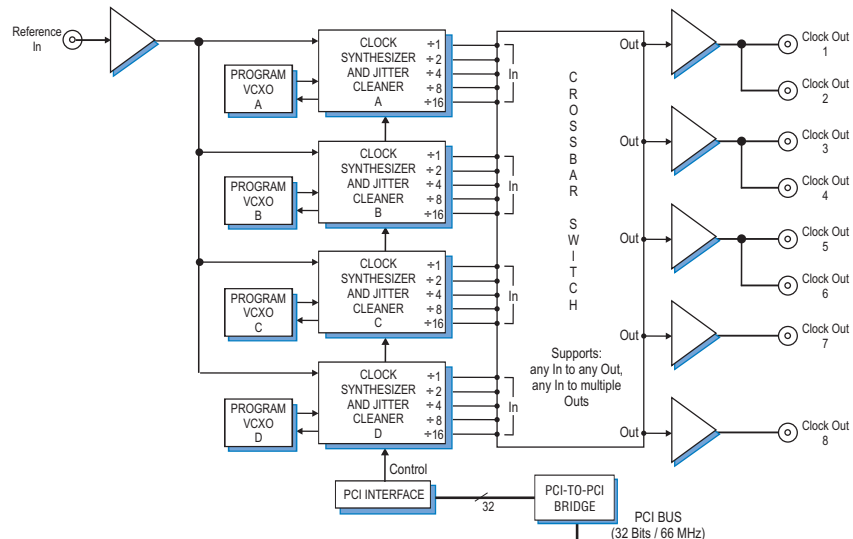
Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board

ReadyFlow
Board Support Package

Ordering Information

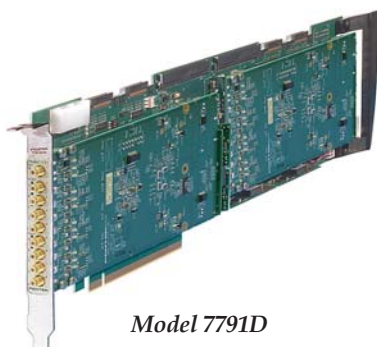
Model	Description
7691	Programmable Multifrequency Clock Synthesizer - PCI



New!

Models 7791, 7791D

Programmable Multifrequency Clock Synthesizers - x16 PCIe



Model 7791D

Features

- Simultaneous synthesis of five or ten different clocks
- Eight or 16 SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

General Information

These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. Model 7791 generates eight clocks while Model 7791D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO (Voltage Controlled Crystal Oscillator) to provide the base frequency for the clock synthesizer. Each of the VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 or 40 frequencies to the board's output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five or ten clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to 16 different clocks to various outputs.

With independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where more than ten different clock outputs are required simultaneously, multiple 7791D's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

These Models include a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four or eight

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: 4 or 8)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: +3 dBm @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port to PCI bus, one x16 port to PCIe motherboard

Operation: control and status interface

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

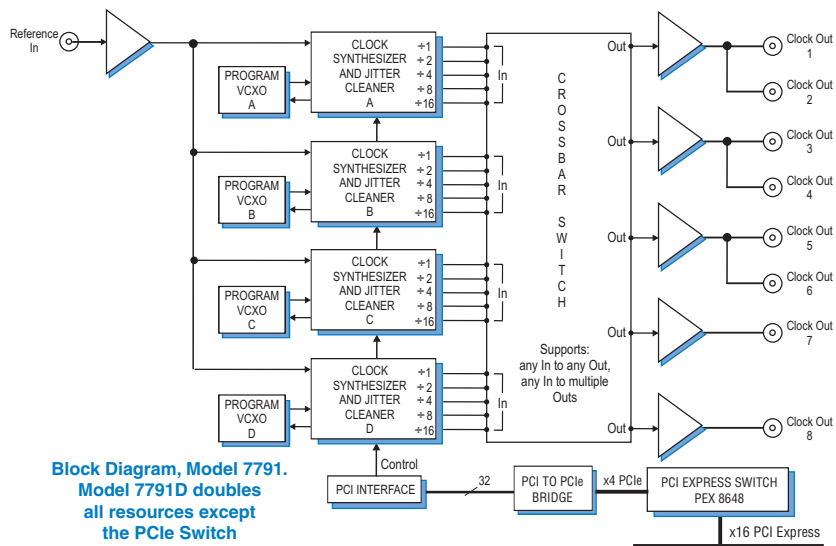
Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.



Ordering Information

Model	Description
7791	Programmable Multifrequency Clock Synthesizer - Full-length x16 PCIe
7791D	Dual Programmable Multifrequency Clock Synthesizer - Full-length x16 PCIe



Block Diagram, Model 7791.
Model 7791D doubles
all resources except
the PCIe Switch

New!

Model 7891

Programmable Multifrequency Clock Synthesizer - x8 PCIe



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

General Information

Model 7891 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7891 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7891 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7891's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

The Model 7891 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10$ dBm

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: Four)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: ± 20 ppm

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3$ dBm @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface

PCIe Interface: Gen. 2, x8 width

PCIe Ports: one x4 port to PCI bus, one

x8 port to PCIe motherboard

Operation: control and status interface

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

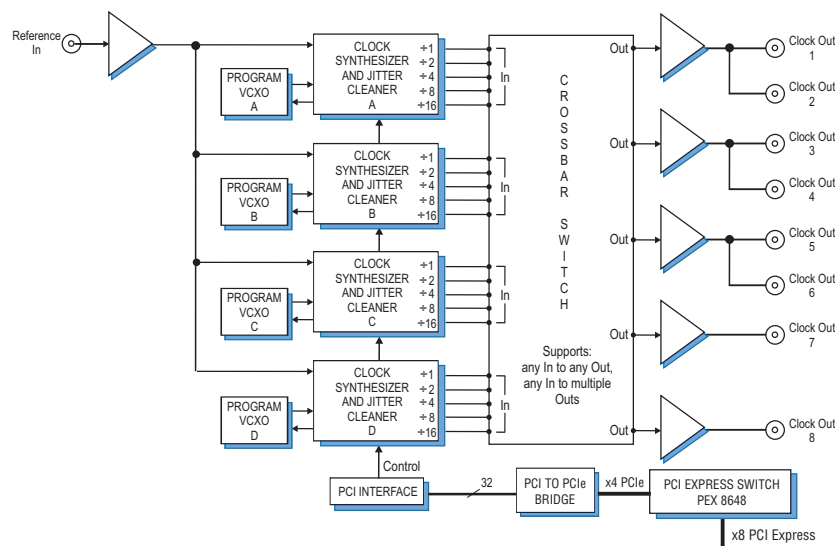
Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

ReadyFlow
Board Support Package

Ordering Information

Model	Description
7891	Programmable Multifrequency Clock Synthesizer - Half-length x8 PCIe



New!

Model 5391

Programmable Multifrequency Clock Synthesizer - 3U VPX



Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane



Ordering Information

Model	Description
5391	Programmable Multifrequency Clock Synthesizer - 3U VPX

General Information

Model 5391 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 5391 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 5391 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of provid-

ing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 5391's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

Model 5390 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to $+10 \text{ dBm}$

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: Four)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: $\pm 20 \text{ ppm}$

Front Panel Clock Outputs (Quantity: Eight)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: $+3 \text{ dBm}$ @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

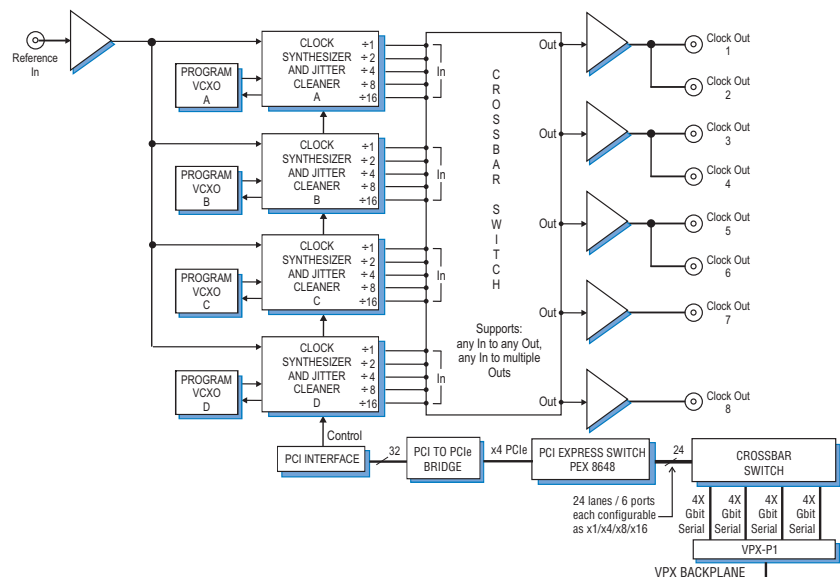
Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)





Features

- Synchronizes up to 80 I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Synchronizes local oscillator phase, decimation phase and frequency switching for multichannel digital receivers and upconverters
- Clock rates up to 105 MHz
- Supports most popular I/O modules
- Front panel SMA connectors for external clock and timing signal inputs and outputs
- 19-inch wide, 1.75 in. high rack-mount chassis with integral AC line power supply
- Flexible cable installation supports many different system configurations

General Information

Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

Input Signals

Clock and timing signals can come from six front panel SMA inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the 9190.

Supported Products

Model 9190 currently supports VIM Models 6210, 6211, 6216, 6228, 6229, 6230, 6231, 6232, 6235, 6236; the PMC Models 7131, 7140, 7141, 7142 and 7150; the PCI Models 7631A, 7640, 7641, 7642 and 7650; and the cPCI Models 7231, 7331, 7240, 7340, 7241, 7341, 7242, 7342 and 7350. Contact us for an up-to-date list of supported modules.

Output Signals

The front panel clock and sync connectors in the list of supported modules fall into two classes, thus requiring two types of front panel cable. The first type uses a 26-pin connector (for the 621x series, the 6229, the 7x31, 7x40 and 7x42 series) delivering the clock and four timing signals. The second type uses a 36-pin connector (for the 623x series) delivering the clock and five timing signals.

Either cable type can be installed in any of the 80 positions of the Model 9190, however, systems with mixed types of I/O modules may not have all functions supported. Contact the factory for assistance with your specific configuration.

Buffered versions of the clock and five timing signals are also available as outputs on the 9190's front panel SMA connectors.

Physical Characteristics

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.

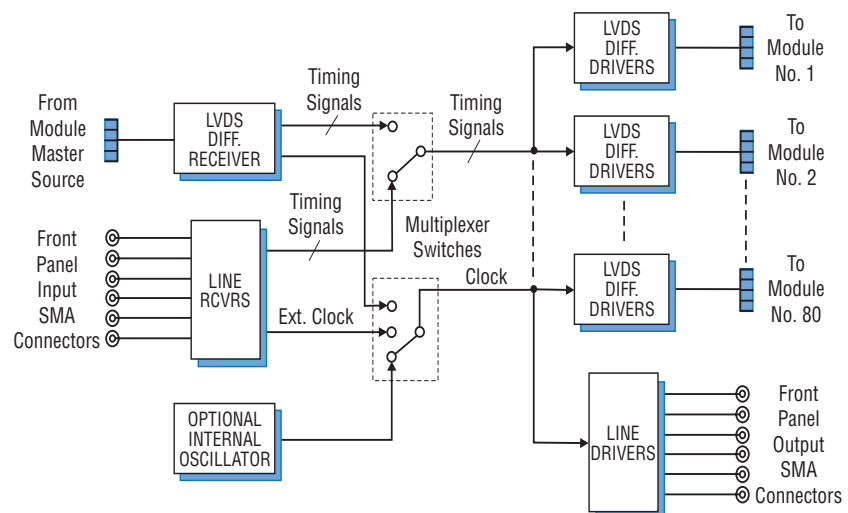
Due to the numerous configuration possibilities allowed by the 9190, Pentek configuration services are required with its purchase.

Ordering Information

Model	Description
9190	Clock and Sync Generator

Options:

-019	64 MHz internal oscillator
-040	40-Channel version





PENTEK

SOFTWARE & FPGA TOOLS

SOFTWARE & FPGA TOOLS

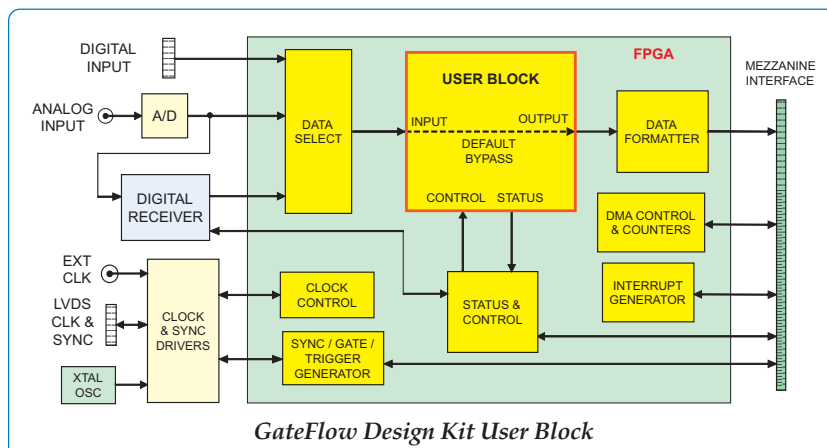
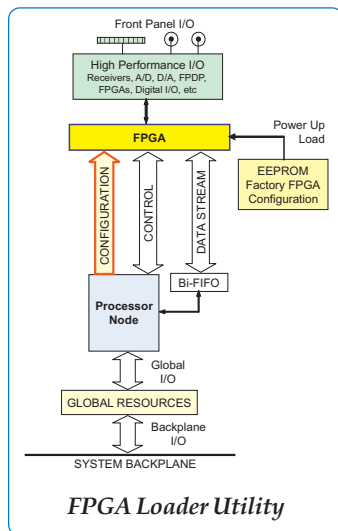
MODEL	DESCRIPTION
4953	Pentek GateFlow® FPGA Design Kit
GateFlow	Pentek GateFlow FPGA Factory-Installed IP Cores
4999	Pentek ReadyFlow® Board Support Package
4994A	Pentek ReadyFlow BSPs for Linux
4995A	Pentek ReadyFlow BSPs for Windows®
4990	Pentek SystemFlow® Recording Software
4977	TI Code Composer Studio with SwiftNet for C6000
VxWorks	Wind River Workbench/VxWorks for PowerPC
4996	Pentek VxWorks BSPs and Drivers
4986	Verari Systems Software VSI/Pro for PowerPC
	Customer Information

Last updated: November 2010



GateFlow is Pentek's family of extendable FPGA products. The GateFlow product line includes the *GateFlow FPGA Design Kit* to ease custom algorithm development and the *GateFlow Factory-installed IP Cores* in Pentek FPGA board products.

For the latest GateFlow information go to: pentek.com/fpga



The Pentek Model 4953 GateFlow FPGA Design Kit provides the user with design information, software files and utilities for extending FPGA functions in these products. Users can implement a variety of custom preprocessing functions such as convolution, framing, pattern recognition, decompression, FFT, delay, beamforming, decoding, time stamping, averaging, and summation.

What's included in the Design Kit

Each Model 4953 GateFlow FPGA Design Kit includes the following:

- The software project used in Xilinx Foundation to create all the standard factory functions of the product including device and bus interfaces, data formatting, clocking, and control
- All VHDL source code modules for the standard factory configuration
- Instructions and utilities for loading a new user-defined configuration to the FPGAs via serial download, parallel upload from the baseboard processor, or custom EEPROM configuration
- Instructions for implementing a software FPGA project

Using the FPGA Design Kit

The GateFlow FPGA Design Kit is intended for the programming of predefined user blocks located in the data flow path specifically reserved for custom applications. These predefined blocks protect users from inadvertently altering base functionality.

Pentek recommends user programming be limited to the predefined user blocks to maintain base functionality. However, for more complex requirements, sufficient information is supplied in the kit for the user to modify, add to, or replace default board functions if necessary. Default configuration files are included with the Design Kit should it be necessary to restore standard factory configuration.

FPGA Design Kit User Block

Shown on this page is the block diagram of a typical software radio module. The diagram includes the FPGA and external hardware devices connected to it.

The blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces. The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control and clocks.

In the standard Design Kit product, the User Block is configured as a straight wire between the input and output ports. By creating a custom algorithm inside the block that conforms to the pin definition, the user will have a low-risk experience in recompiling and installing the custom code. Since Pentek provides source code for all the modules, changes outside the user block can also be made by the user.

FPGA Design Kit Project Files

The GateFlow Design Kit is intended for use with the Xilinx ISE Foundation Tool Suite. The user should be trained in and be familiar with this tool and general FPGA design principles.

The Design Kit installs as a complete project file within the ISE environment and includes all the project files that Pentek engineers used to create the standard product. Included are configuration and definition files, VHDL source code, JTAG definition files and I/O block diagrams. The FPGA Design Kit also includes several helpful utilities and a very important resource, the FPGA Loader Utility.

FPGA Design Kit Loader Utility

Normally, the FPGA is loaded from a nonvolatile EEPROM with the standard factory configuration code when the product is powered up.

The FPGA Loader Utility allows the processor associated with the FPGA product to reconfigure the FPGA as a software task, effectively overwriting the factory configuration code. As a result, there is no need to turn off power, no need to disassemble the board or system and no need to attach any special cables or harnesses to the board.

The FPGA can be reconfigured in this manner during initialization to install custom operational modes and features. It can also facilitate product upgrades and enhancements that can dramatically extend product longevity.



Xilinx FPGAs in Pentek Products

The charts below show the Xilinx FPGA families as used in the various Pentek board-level products.

These products use some FPGA resources to implement standard factory functions and installed IP cores in some cases.

Since many of the newer FPGAs are so large, even after all these functions have been implemented, a significant percentage of

FPGA resources remain unused and available for customer use.

The charts show the percentage of unused system slices and RAM available to the user for extending the FPGA to include custom algorithms.

Shown in the next page is ordering information for selecting and specifying the desired Model 4953 FPGA Design Kit Option number for current Pentek products.

			Available FPGA Resources for Pentek Hardware											
			Xilinx Virtex-II Pro				Xilinx Virtex-4							
			-VP50		-VP70		-FX60		-FX100		-SX55		-LX100	
Logic Cells			53,136		74,448		56,880		94,986		55,296		110,592	
CLB Slices			23,616		33,088		25,280		42,176		24,576		49,152	
CLB Flip-Flops			47,232		66,176		50,560		84,352		49,152		98,304	
Max. Block RAM			4,176 k		5,904 k		4,176 k		6,768 k		5,760 k		4,320 k	
Multipliers / DSP Blocks			232		328		128		160		512		96	
PowerPCProcessorBlocks			2		2		2		2		–		–	
Pentek Model	Board Type	No. of FPGAs	% Available to User				% Available to User							
			Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM
4207	VME/VXS	1	–	–	–	–	38%	71%	61%	82%	–	–	–	–
6251	VIM-2	2	99%	100%	–	–	–	–	–	–	–	–	–	–
6256	VIM-2	2	98%	100%	–	–	–	–	–	–	–	–	–	–
6821	VME/VXS	2	98%	100%	–	–	–	–	–	–	–	–	–	–
6822	VME/VXS	2	98%	100%	–	–	–	–	–	–	–	–	–	–
6826	VME/VXS	1	–	–	75%	72%	–	–	–	–	–	–	–	–
7140*	PMC/XMC	1	55%	72%	–	–	–	–	–	–	–	–	–	–
7141*	PMC/XMC	1	55%	72%	–	–	–	–	–	–	–	–	–	–
7142*	PMC/XMC	2	–	–	–	–	77%	92%	86%	95%	54%	78%	77%	71%

			Available FPGA Resources for Pentek Hardware																	
			Xilinx Virtex-5						Xilinx Virtex-6											
			-SX50T		-SX95T		-LX155T		-LX130T		-LX240T		-LX365T		-SX315T		-SX475T			
Logic Cells			52,224		94,208		155,648		128,000		241,152		364,032		314,880		476,160			
CLB Slices			8,160		14,720		24,320		20,000		37,680		56,880		49,200		74,400			
CLB Flip-Flops			32,640		58,880		97,280		160,000		301,440		455,040		393,600		595,200			
Max. Block RAM			4,752 k		8,784 k		7,632 k		1,740 k		3,650 k		4,130 k		5,090 k		7,640 k			
Multipliers / DSP Blocks			288		640		128		480		768		576		1,344		2,016			
PowerPC Processor Blocks			–		–		–		–		–		–		–		–			
Pentek Model	Board Type	No. of FPGAs	% Available to User								% Available to User									
			Slices		RAM		Slices		RAM		Slices		RAM		Slices		RAM		Slices	
7150*	PMC/XMC	2	7%	75%	36%	86%	64%	84%	–	–	–	–	–	–	–	–	–	–	–	–
7153*	PMC/XMC	2	N/A	N/A	42%	45%	N/A	N/A	–	–	–	–	–	–	–	–	–	–	–	–
7156*	PMC/XMC	2	16%	59%	50%	78%	69%	74%	–	–	–	–	–	–	–	–	–	–	–	–
7158*	PMC/XMC	2	16%	59%	50%	78%	69%	74%	–	–	–	–	–	–	–	–	–	–	–	–
71620*	XMC	1	–	–	–	–	–	–	61%	66%	79%	79%	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
71660*	XMC	1	–	–	–	–	–	–	61%	66%	79%	79%	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

* Other form factors: 72XX = 6U cPCI; 73XX = 3U cPCI; 76XX = PCI; 77XX = Full-Length PCIe; 78XX = Half-Length PCIe; 53XX = 3U VPX

% Available to User: Applies to the Processing FPGA(s); % Available can vary slightly due to rounding

Ordering Information

Model	Description
4953	GateFlow FPGA Design Kit

Options: Supported Product w/
FPGA option

-131-030*	7131 w/ XC2V3000
-140-052*	7140 w/ XC2VP50
-141-052*	7141 w/ XC2VP50
-142-055*	7142 w/ XC4VSX55
-142-060*	7142 w/ XC4VFX60
-142-100*	7142 w/ XC4VFX100
-142-110*	7142 w/ XC4VLX100
-150-083*	7150 w/ XC5VLX155T
-150-084*	7150 w/ XC5VSX50T
-150-085*	7150 w/ XC5VSX95T
-153-085*	7153 w/ XC5VSX95T
-156-083*	7156 w/ XC5VLX155T
-156-084*	7156 w/ XC5VSX50T
-156-085*	7156 w/ XC5VSX95T
-158-083*	7158 w/ XC5VLX155T
-158-084*	7158 w/ XC5VSX50T
-158-085*	7158 w/ XC5VSX95T
-620-061*	71620 w/ XC6VLX130T
-620-062*	71620 w/ XC6VLX240T
-620-063*	71620 w/ XC6VLX365T
-620-064*	71620 w/ XC6VSX315T
-620-065*	71620 w/ XC6VSX475T
-660-061*	71660 w/ XC6VLX130T
-660-062*	71660 w/ XC6VLX240T
-660-063*	71660 w/ XC6VLX365T
-660-064*	71660 w/ XC6VSX315T
-660-065*	71660 w/ XC6VSX475T

Options: Supported Product w/
FPGA option

-205-010	4205 w/ XC2V1000
-205-030	4205 w/ XC2V3000
-207-060	4207 w/ XC4VFX60
-207-100	4207 w/ XC4VFX100
-228-010	6228 w/ XC2V1000
-228-030	6228 w/ XC2V3000
-230-006	6230 w/ XCV600E
-231-006	6231 w/ XCV600E
-232-006	6232 w/ XCV600E
-235-010	6235 w/ XC2V1000
-235-030	6235 w/ XC2V3000
-236-010	6236 w/ XC2V1000
-236-030	6236 w/ XC2V3000
-250-010	6250 w/ XC2V1000
-250-030	6250 w/ XC2V3000
-251-022	6251 w/ XC2VP20
-251-052	6251 w/ XC2VP50
-256-022	6256 w/ XC2VP20
-256-052	6256 w/ XC2VP50
-821-022	6821 w/ XC2VP20
-821-052	6821 w/ XC2VP50
-822-022	6822 w/ XC2VP20
-822-052	6822 w/ XC2VP50
-826-072	6826 w/ XC2VP70

* Other form factors: 72XX = 6U cPCI; 73XX = 3U cPCI; 76XX = PCI; 77XX = Full-Length PCIe; 78XX = Half-Length PCIe; 53XX = 3U VPX

Example:	Model	Description	Form Factor
	7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	PMC/XMC
	7250	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	6U cPCI
	7350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	3U cPCI
	7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	PCI
	7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	x16 PCIe
	7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	x8 PCIe
	5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	3U VPX

Contact Pentek for the latest products and FPGA options.

New!



GateFlow is Pentek's family of extendable FPGA products. The GateFlow product line includes the *GateFlow FPGA Design Kit* to ease custom algorithm development and the *GateFlow Factory-installed IP Cores* in Pentek FPGA board products.

For the latest GateFlow information go to: pentek.com/fpga



Pentek Factory-Installed IP Cores

Pentek has implemented popular signal processing algorithms as GateFlow factory-installed IP Cores. First, these cores are highly-optimized to take maximum advantage of each Xilinx FPGA family, and then uniquely adapted to the architectures of specific Pentek boards to achieve maximum performance and flexibility. These cores exploit highly-parallel processing structures that dramatically outperform programmable RISC and DSP processors.

Pentek offers a wide range of IP cores including FFTs, DDCs (digital downconverters), and interpolation filters.

Two highly-pipelined 1024- and 4096-point FFT engines are available for various VIM modules. Several wideband DDC cores are available for VIM modules and high speed VME A/D converters. Similar to the TI GC1012B in decimation, they offer enhanced speed and performance.

For PMC modules and derivative PCI, cPCI, PCIe, and VPX products, Pentek offers several IP cores that extend the range of DDCs to handle a wider range of received

baseband signals. Some of these cores add interpolation filters to extend the hardware DUC filter to handle lower bandwidths of transmitted baseband signals.

Pentek's multiband DDC cores handle an extremely wide range of signal bandwidths. For high density DDC systems, Pentek offers a 32-channel multiband DDC, two 256-channel DDCs and a core with beamforming functions. These unique cores dramatically outperform ASIC DDCs by taking full advantage of parallel DSP resources within the FPGA.

All of these IP cores are delivered to you preinstalled in specific Pentek FPGA-based products and are fully supported with Pentek ReadyFlow Board Support Packages. Purchasing these popular factory-installed cores saves you the time and costs of acquiring FPGA tools and developing custom FPGA code.

Custom Design Services

For qualified opportunities, Pentek IP cores or modified versions can be installed in Pentek hardware. Please contact Pentek Sales to discuss your needs.

VIM Modules with FFT Cores

- Model 6235-401: Dual 12-bit A/D and Wideband DDC with Dual 1k FFT Core
- Model 6235-404: Dual 12-bit A/D and Wideband DDC with Dual 1k FFT Core
- Model 6250-404: Configurable Logic FPGA and FPDP I/O with Dual 4K FFT Core

VIM Modules with Wideband DDC IP Cores

- Model 6235-421: Dual 12-bit A/D with Dual Wideband DDC Core
- Model 6236-421: Dual 14-bit A/D with Dual Wideband DDC Core

VME/VXS Boards with Wideband DDC IP Cores

- Model 6821-422: 215 MHz A/D with Wideband DDC Core

PMC/XMC, PCI, cPCI, PCIe and VPX Boards with DDC & DUC IP Cores

- Model 7X40-420: Transceiver with Multiband DDC & Interpolation Filter Core
- Models 7X41-420, 5341-420: Transceivers with Multiband DDC & Interpolation Filter Cores
- Models 7X42-428, 5341-428: Transceivers with Multiband DDC & Interpolation Filter Cores

PMC/XMC, PCI, cPCI, PCIe and VPX Boards with 256-Channel DDC IP Cores

- Model 7X40-430: Transceiver with 256-Ch Narrowband DDC Core
- Models 7X41-430, 5341-430: Transceivers with 256-Channel Narrowband DDC Cores
- Models 7X51, 5351: Quad 200 MHz A/D with 256-Channel DDC Cores

PMC/XMC, PCI, cPCI, PCIe and VPX Boards with 32-Channel DDC IP Cores

- Models 7X52, 5352: Quad 200 MHz A/D with 32-Channel Multiband DDC Core

PMC/XMC, PCI, cPCI, PCIe and VPX Boards with 4/2-Channel DDC IP Cores

- Models 7X53, 5353: Quad 200 MHz A/D with 4/2-Channel DDC and Beamformer Cores

Products that are available in several form factors:

- 71XX: PMC/XMC Modules
- 72XX: 6U CompactPCI Boards
- 73XX: 3U Compact PCI Boards
- 76XX: PCI Boards
- 77XX: Full-length PCI Express Boards
- 78XX: Half-length PCI Express Boards
- 53XX: 3U VPX Boards

For the latest list of boards supported with ReadyFlow, visit our website at:
www.pentek.com/readyflow



What Development Environments are Supported?

The ReadyFlow Board Support Package for C6000 processor boards is written to work seamlessly with the Texas Instruments DSP/BIOS real-time kernel which is included free of charge with TI's Code Composer Studio.

Developers using PowerPC-based embedded processor boards have traditionally used either Wind River's VxWorks environment, supported by the Pentek Model 4996 VxWorks Board Support Package, or a Linux environment. ReadyFlow offers an additional option: integrated support for eCos, an open source, royalty-free, real-time operating system intended for embedded applications.

eCos-based applications can be developed with GNU open source development tools including the GCC C-language compiler, GDB debugger and Insight GUI interface for GDB. ReadyFlow packages for PowerPC-based processor boards include the board support package, a complete distribution of eCos, GNU code development tools, complete documentation and example applications.

Users of card-cage based instrumentation often find themselves frustrated by the fact that when their new devices are delivered, they are unable to put them to immediate use. Because these instruments are largely software controlled, a certain amount of programming is generally necessary in order to put the new cards through their paces. Then, if something does not go as planned, there is no way of knowing for sure whether the problem lies with the new code you've written, or with the hardware itself.

To address this issue, Pentek has developed the **ReadyFlow** Board Support Package for all its board-level products. These packages:

- Provide development tools for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete source code for all board functions
- Include complete documentation and definitions of all functions

What's Included in the Package

In general, functions appropriate to the board-level product, such as:

- A "How to" section
 - Build object libraries
 - Compile and link application programs
- C-callable functions
 - Initialization and test
 - Data movement and communications
 - Backplane I/O
 - Mezzanine peripheral I/O
 - Control of board resources
- Utilities
 - Flash memory program loaders

The package contains C-language examples that can be used to demonstrate the capabilities of Pentek products. The examples included provide the answers to most of the questions that occur with first-time users of our products. These programming examples will also help you get an immediate start on writing your own application without having to reinvent the wheel. They provide sample code that is known to work, giving you, the new user, a means of verifying that your board set is operational.

ReadyFlow Board Support Packages are designed to reduce development time not only during the initial stages, but any time new hardware is added to the system. All packages are built with a consistent style and function naming convention. Similar parameters on different boards have similar function calls, thereby allowing immediate familiarity with new hardware as it's added, further shortening the learning curve.

Example, Model 4205 Processor

As an example of a processor board, the Model 4205 package includes support for the following:

- Real-time kernel
- Choice of schedulers
- Thread support
- Synchronization primitives
- Timers, counters and alarms
- Memory allocation
- Debug and instrumentation support
- Interrupt and exception handling
- ISO C and math libraries
- Serial and Ethernet device drivers
- Wallclock device drivers
- TCP/IP networking stacks
- GDB debug support
- SCSI device support over Fibre Channel

Example, Model 7141

As an example of a PMC module, the Model 7141 software radio transceiver package includes data structures and routines to support the following:

- PCI Bus interface and DMA controller
- Board control registers
- Endianness control
- Timing bus control and clock selection
- Triggering, gate enable and polarity
- Data input device management for the A/D and the GC4016 DDC
- Data output device management for the DAC5686 D/A and the DUC
- Delay memory operation
- Interrupt generation and handling
- FPGA configuration
- Test modes and hardware revision codes
- Hardware voltage and temperature monitor ➤

► Embedded Configurable Operating System (eCos)

ReadyFlow offers PowerPC software developers a powerful new option for embedded application development. ReadyFlow includes integrated support for eCos, an open source, royalty-free, real-time operating system intended for embedded applications. As an alternative to costly operating systems, eCos-based applications can be developed with free GNU open source development tools including the GCC C-language compiler, GDB debugger and Insight GUI interface for GDB.

ReadyFlow packages for PowerPC based processor boards include an eCos enabled board support package, a complete distribution of eCos, GNU code development tools, complete documentation and example applications.

eCos Core Components

Designed as a full-featured, real-time operating system, eCos delivers a complete suite of functions needed in many embedded applications including:

Hardware Abstraction Layer (HAL) - provides a software layer that gives access to hardware.

Kernel - includes interrupt and exception handling, thread and synchronization support, a choice of scheduler implementations, timers, counters and alarms.

ISO C and Math Libraries - provide standard compatibility with function calls.

Device Drivers - include standard serial, Ethernet, Flash ROM, and others.

eCos Features

- Real-time performance
- Low interrupt latency
- Low task switching latency
- Small memory footprint
- Deterministic behavior
- Highly configurable
- Full feature set
- Open source kernel
- No runtime licensing, fees or royalties
- Open source GNU development tools

GDB support - provides target software for communication with a GDB host enabling application debugger.

eCos is Highly Configurable

A key feature of eCos is its highly configurable design. The kernel is scalable to include only the components needed for a specific application, allowing a small efficient footprint for simple applications, or a full-featured configuration for more complex systems. In addition, eCos can be built without an actual kernel for applications that might not need multitasking, further reducing the memory footprint and improving execution speed.

eCos configuration is performed through the graphical configuration tool shown below. The user interface displays the properties of each component including parameters, switches, sizes, component description, etc. thereby allowing developers to easily rebuild the kernel as needed.

Kernel Benchmarks

Applications developed with eCos can benefit from excellent kernel run time performance. Below are timing benchmarks generated on the Model 4205 MPC7457 I/O processor board running at 1 GHz and configured with a 2 Mbyte L3 cache:

<u>Function</u>	<u>Average Time (usec)</u>
Thread Switch	0.59
Put or Get Mailbox	0.29
Mailbox Put/Get	0.77
Post Semaphore	0.14
Wait Semaphore	0.16
Post/Wait Semaphore	0.80
Wait for Flag [AND]	0.21



Ordering Information

Model	Description
4994A	Pentek ReadyFlow BSPs for Linux

The Pentek ReadyFlow BSPs for Linux provide developers with a complete interface for hardware initialization, control and application functions for PMC and XMC modules, as well as VME/VXS PowerPC baseboards. Each BSP's familiar Linux interface includes programming examples to speed application development. Baseboard BSPs support the standard Linux kernel.

The BSPs are designed to reduce development time, not only during the initial stages of software development, but any

time new I/O hardware is added to the system. PMC BSP libraries, each designed to control the specific hardware features of the I/O interface being used, are built with a consistent style and parameter-naming convention. Similar parameters on different I/O modules have similar library calls, thereby allowing immediate familiarity with hardware as it's added. This can greatly shorten the application development learning curve when a system is modified or expanded.

The Pentek ReadyFlow BSPs for Windows provide developers with a complete library of hardware initialization, control and application functions for PMC and XMC modules. The BSPs include C-language device libraries as well as high-level APIs and programming examples to speed application development, and to allow developers the level of hardware access appropriate for their specific application.

The BSPs are designed to reduce development time, not only during the initial

stages of software development, but any time new I/O hardware is added to the system. The BSP libraries, each designed to control the specific hardware features of the I/O interface being used, are built with a consistent style and function-naming convention. Similar parameters on different I/O modules have similar library calls, thereby allowing immediate familiarity with hardware as it's added. This can greatly shorten the application development learning curve when a system is modified or expanded.

Ordering Information

Model	Description
4995A	Pentek ReadyFlow BSPs for Windows

Ordering Information

Model Description

4995A Pentek ReadyFlow BSPs for Windows

Options Description

-140 For Model 7x40
 -140-420 For Model 7x40 with IP Core 420 installed
 -140-430 For Model 7x40 with IP Core 430 installed
 -141 For Model 7x41
 -141-420 For Model 7x41 with IP Core 420 installed
 -141-430 For Model 7x41 with IP Core 430 installed
 -142 For Model 7x42
 -142-428 For Model 7x42 with IP Core 428 installed
 -150 For Model 7x50
 -151 For Model 7x51
 -152 For Model 7x52

The "x" designation in the model number descriptions refers to the form factor of the board as follows:

x Form Factor
 1 PMC or XMC
 2 6U CompactPCI
 3 3U CompactPCI
 6 PCI
 7 Full-Length PCI Express
 8 Half-Length PCI Express



Features

- Complete turnkey recording and/or playback system software for RTS systems
- Software API for controlling data acquisition and recorder functions
- Graphical user interface
- Windows or Linux host
- Storage up to 4 terabytes
- One-year support included

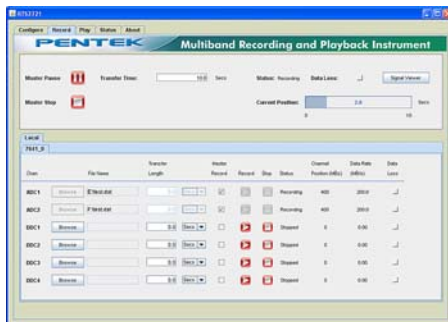
General Information

The Model 4990 SystemFlow Recording Software provides a rich set of function libraries and tools for controlling and building Pentek's RTS real-time recording and data acquisition systems. These libraries ensure a consistent look and feel for developers across RTS system families. SystemFlow software allows developers to configure and customize system interfaces and behavior. It includes API functions not only for the real-time data acquisition and playback functions, but also for the user-control software running on the host PC including the GUI. These API functions allow developers to either modify the sample code to meet their needs or use it as a reference for custom software development.

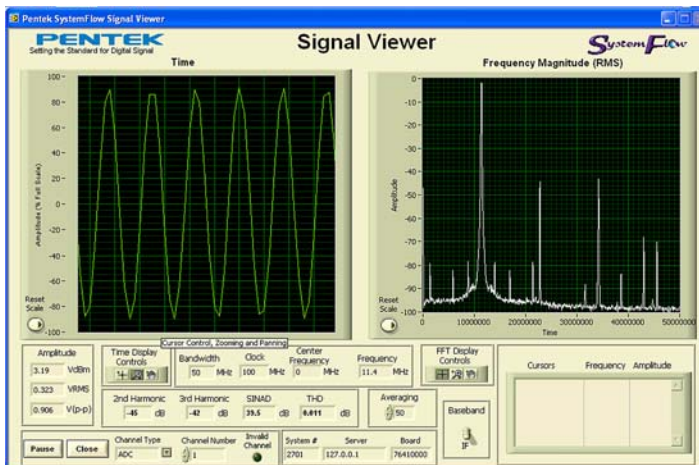
API Library Components

SystemFlow is based on a flexible client/server architecture. The host client application runs on a Windows or Linux platform and communicates with the server target application via a standard socket connection. In this way, server real-time recording and/or playback operations can be controlled from a local or remote host client.

All RTS servers use PC hardware running under Windows. The server application includes scheduling, task management, full control of data from Pentek software radio hardware, and drivers for communication with the hard disk arrays.



Recorder Interface



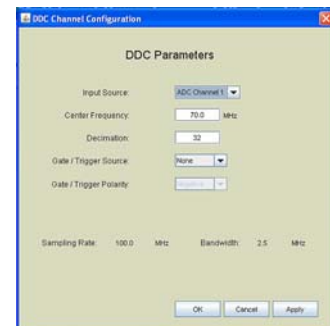
Signal Viewer

SystemFlow Recorder Interface

The SystemFlow GUI provides the user with a control interface for recording data. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

Hardware Configuration Interface

The SystemFlow configuration screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.



Hardware Configuration Interface

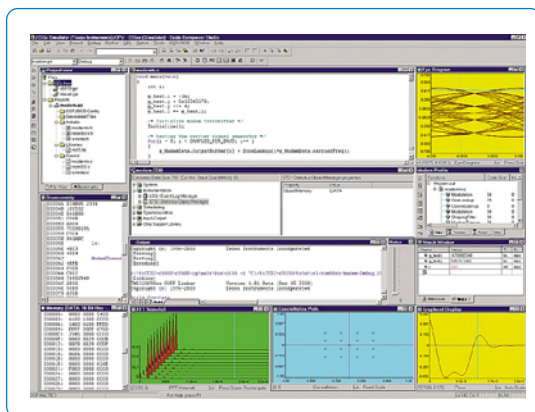
SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

More information on pentek.com

Model 4977 consists of **Code Composer Studio** packaged with **SwiftNet** Host Networking and Communication software. Code Composer Studio is a fully integrated development environment (IDE) which provides a



menu-driven graphical interface for the debugging and networking capabilities of SwiftNet. It integrates system debuggers, signal probes, and other tools into one Windows environment that supports TI's C6000 DSP processor family.

Aimed specifically at DSP development, this software package offers advanced features that allow designers to edit, build, debug, profile and manage

projects from a single unified environment. In addition, it lets users compile in the background and analyze signals graphically.

Code Composer Studio seamlessly interfaces to the numerous debugging and networking features of SwiftNet software. Networking and communication capabilities added by SwiftNet include access to multiple DSP chips on a single multiprocessor board, multiple workstation access to a single VMEbus card cage, simultaneous debugging of multiple processors by different users, and DSP development over the internet, intranet or networks.

Although the C6000 can achieve in excess of 5000 MIPS, the effective MIPS figure depends on the level of instruction parallelism and data throughput that can be achieved, which is determined by the software. The integrated profiler and other features in Code Composer Studio can help designers develop more complex, optimized code to fully exploit the resources of the C6000 for maximum performance.

Model 4977 provides a complete DSP developer's package, combining the essential tools of Code Composer Studio with SwiftNet's powerful connectivity and debugging capabilities. This software package presently supports Windows 98/NT/2000/XP for all Pentek C6000 processor boards. For more information on SwiftNet and its features, see Pentek Model 4945 SwiftNet Host Software.

Pentek embraces Texas Instruments' eXpressDSP™ real-time software development environment including such products as the DSP/BIOS and Code Composer Studio plug-ins.

DSP/BIOS is a scalable real-time kernel designed for C6000 DSPs and applications requiring real-time scheduling and synchronization. Its open plug-in environment makes Code Composer Studio easily adaptable to different development needs.

The **SwiftNet Debug Manager plug-in** provides seamless integration between Code Composer Studio and SwiftNet's debugging capability. The SwiftNet Debug Manager plugs into the Code Composer Studio setup program. It simplifies the setup process, allowing the user to specify all the processors in a system with user defined names. Based on the user's input, the plug-in adds the appropriate processor information into Code Composer Studio's setup allowing the software developer to open as many debug windows as DSPs in the system.

Once the hardware information has been entered using the SwiftNet Debug Manager, the **SwiftNet Project plug-in** determines all the project settings required by Code Composer Studio and passes these parameters to the program. Information like directories, linker command files, and compiler switch settings are automatically loaded, thereby allowing developers to start working immediately on the application.

Ordering Information

Model	Description
4977	Code Composer Studio with SwiftNet for C6000
Option:	
-100	Complete Package for Windows 98/NT/2000/XP (includes code generation and debugging tools)

Ordering Information

Contact Wind River Systems at:
www.windriver.com

Wind River's **Workbench** development platform has dramatically improved embedded developers' "time-to-productivity". A component of Workbench, Workbench Tools, comprises a comprehensive suite of core and optional cross-development tools and utilities. The other integrated components of Workbench consist of the VxWorks run-time system, a high-performance scalable real-time operating system that executes on the target processor and a full range of communications options for the target connection to the host. Workbench Tools provides a

highly visual and automated environment that accelerates the development of even the most complex VxWorks-based applications.

At the heart of the VxWorks run-time system is the highly efficient Wind microkernel which supports a full range of real-time features. These include fast multitasking, interrupt support, and both preemptive and round-robin scheduling. The microkernel design minimizes system overhead and enables fast, deterministic response to external events.



Ordering Information

Model	Description
4996	Pentek VxWorks BSPs and Drivers

The Model 4996 **VxWorks BSP** provides software developers with a complete library of hardware initialization, control and application functions for Pentek G4 PowerPC processor baseboards and VIM and PMC modules. Used in conjunction with Wind River’s **Workbench** software development environment, it speeds application development by providing a high-level API for accessing all of the processor board’s memory and communication resources, and control of the board’s I/O interfaces and I/O modules.

Processor specific functions found in the baseboard BSPs include: cache, DMA, SDRAM, interrupt, serial port, and timer control. Some general board functions include: reading and writing to mezzanine board FIFOs, VIM and PMC I/O control, interprocessor communication, programming

DMA reads and writes, programming interrupts, using mailboxes, managing RS-232 and ethernet interfaces, and control of optional RACE++ and Fibre Channel interfaces.

The VxWorks BSP is designed to reduce development time not only during the initial stages of software development, but any time new I/O hardware is added to the system. VIM and PMC **Drivers**, each designed to control the specific hardware features of the I/O interface being used, are built with a consistent style and function naming convention. Similar parameters on different I/O modules have similar driver calls, thereby allowing immediate familiarity with new VIM or PMC I/O hardware as it’s added. This can greatly shorten the application development learning curve when a system is modified or expanded.



Ordering Information

Model	Description
4986	Verari Systems Software VSI/Pro

The VSIPL (Vector, Signal and Image Processing Library) standard consists of definitions of over 500 scientific and engineering functions. It supports portable, high performance applications programming.

The standard is based upon existing libraries that have evolved and matured over decades of computing. These include functions for linear algebra, signal processing (FFTs, windowing, filtering and convolution routines), image processing, scalar functionality, and vector and matrix view functionalities (scalar, unary, binary and ternary operations).

The Verari Systems Software **VSI/Pro** is an implementation of VSIPL functions optimized specifically for the PowerPC and AltiVec architectures and is designed to be fully compliant with the emerging VSIPL standard.

As a commercial implementation, VSI/Pro is the immediate step between the VSIPL standard and your own specialized software application. The library is compatible with Wind River's VxWorks real-time operating system and supports the ANSI C and C++ languages.

Customer Information

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When placing purchase orders for Pentek products, please provide the model numbers and descriptions used in this catalog. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

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International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

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Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside of the USA.

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This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

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Before returning a product for service and repair, please contact Customer Service to obtain a Return Material Authorization (RMA) number and have the following information available: model number, serial number, name and address of person returning the product and a description of the problem experienced.

Carefully package the product in its original antistatic material, if it is still available, and ship it to us: prepaid (if within the US) or free domicile DDP (if outside the US). Show the RMA number on the outside of the package and include a written description of the malfunction.

When the work is completed, we will return the product to you free of charge, along with a statement of work done, if under warranty. Out-of-warranty work will be charged on a material and service time basis, and we will be happy to quote you a cost estimate for the repair and return shipping before proceeding.

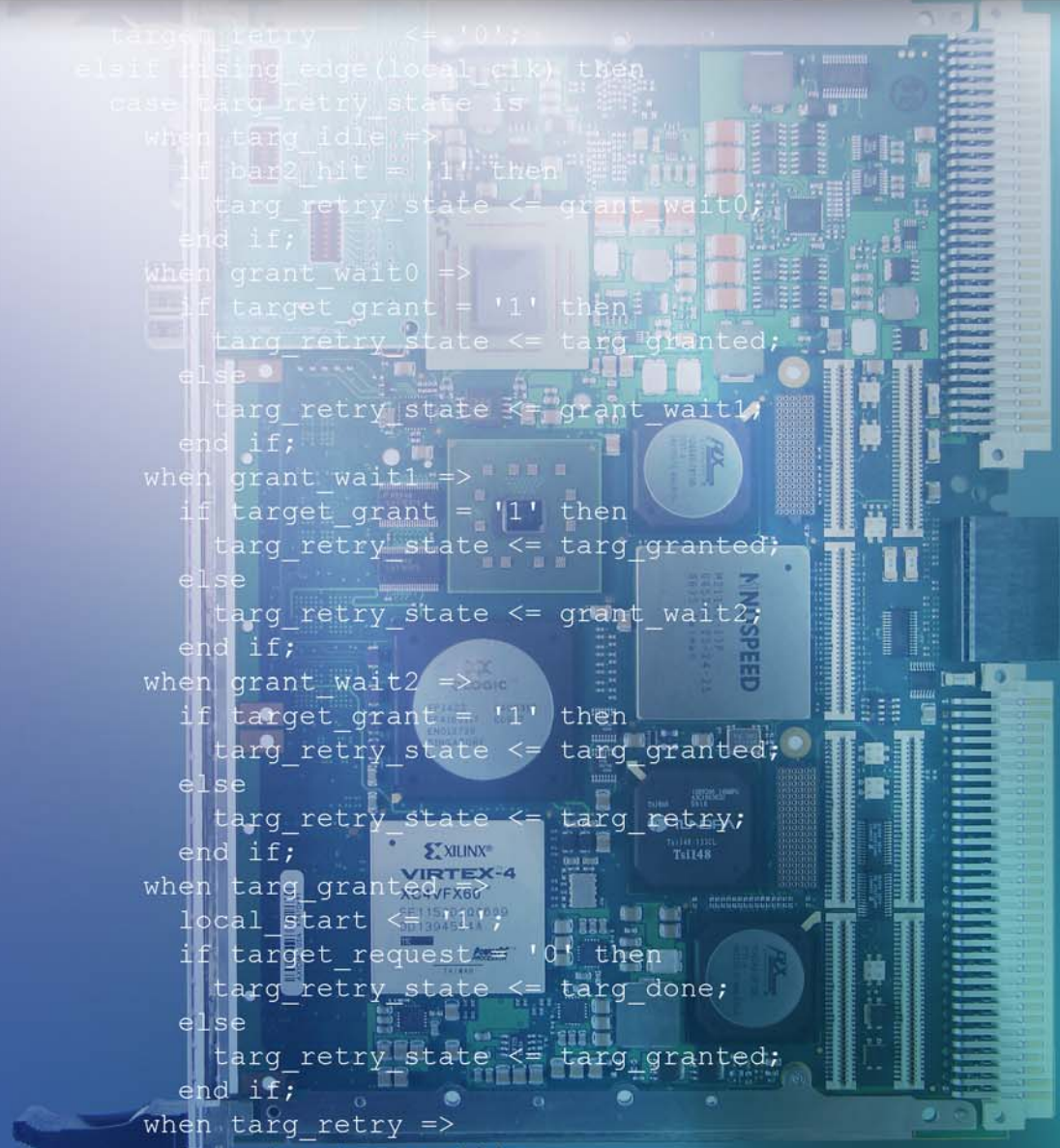
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PRODUCT CATALOG



```
target_retry <= '0';
elsif rising_edge(local_clk) then
  case targ_retry_state is
    when targ_idle =>
      if bar2_hit = '1' then
        targ_retry_state <= grant_wait0;
      end if;
    when grant_wait0 =>
      if target_grant = '1' then
        targ_retry_state <= targ_granted;
      else
        targ_retry_state <= grant_wait1;
      end if;
    when grant_wait1 =>
      if target_grant = '1' then
        targ_retry_state <= targ_granted;
      else
        targ_retry_state <= grant_wait2;
      end if;
    when grant_wait2 =>
      if target_grant = '1' then
        targ_retry_state <= targ_granted;
      else
        targ_retry_state <= targ_retry;
      end if;
    when targ_granted =>
      local_start <= '0';
      if target_request = '0' then
        targ_retry_state <= targ_done;
      else
        targ_retry_state <= targ_granted;
      end if;
    when targ_retry =>
      target_retry <= '1';
      if S_DATA = '1' then
        targ_retry_state <= targ_retry;
```

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